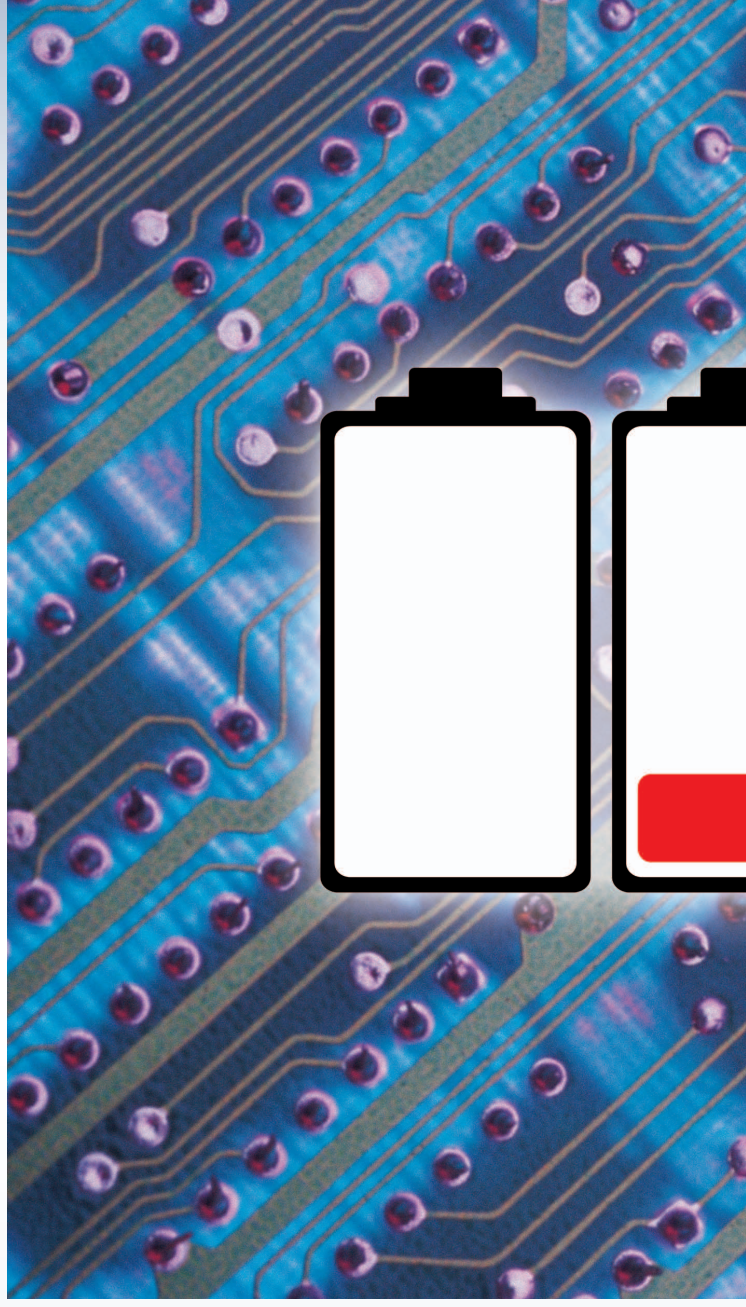
Feature

RF Energy Harvesting for Embedded Systems: A Survey of Tradeoffs and Methodology



Tolga Soyata, Lucian Copeland, and Wendi Heinzelman

Abstract

This paper presents an overview of passive Radio Frequency (RF) energy reception and power harvesting circuits for isolated communications and computing systems lacking access to primary power sources. A unified understanding of the energy harvesting alternatives is provided, followed by an elaborate study of RF energy harvesting within the context of embedded systems. A detailed discussion of RF technologies ranging from the directed communications signal reception to dispersed ambient power harvesting is provided. A comparative focus on design tradeoffs and process alterations is provided to represent the diversity in the applications requiring wireless RF harvesting units. Also included is an analysis of system combinations, and how wake up units, active storage, and duty cycling play roles in the consumption and harvesting of RF energy.

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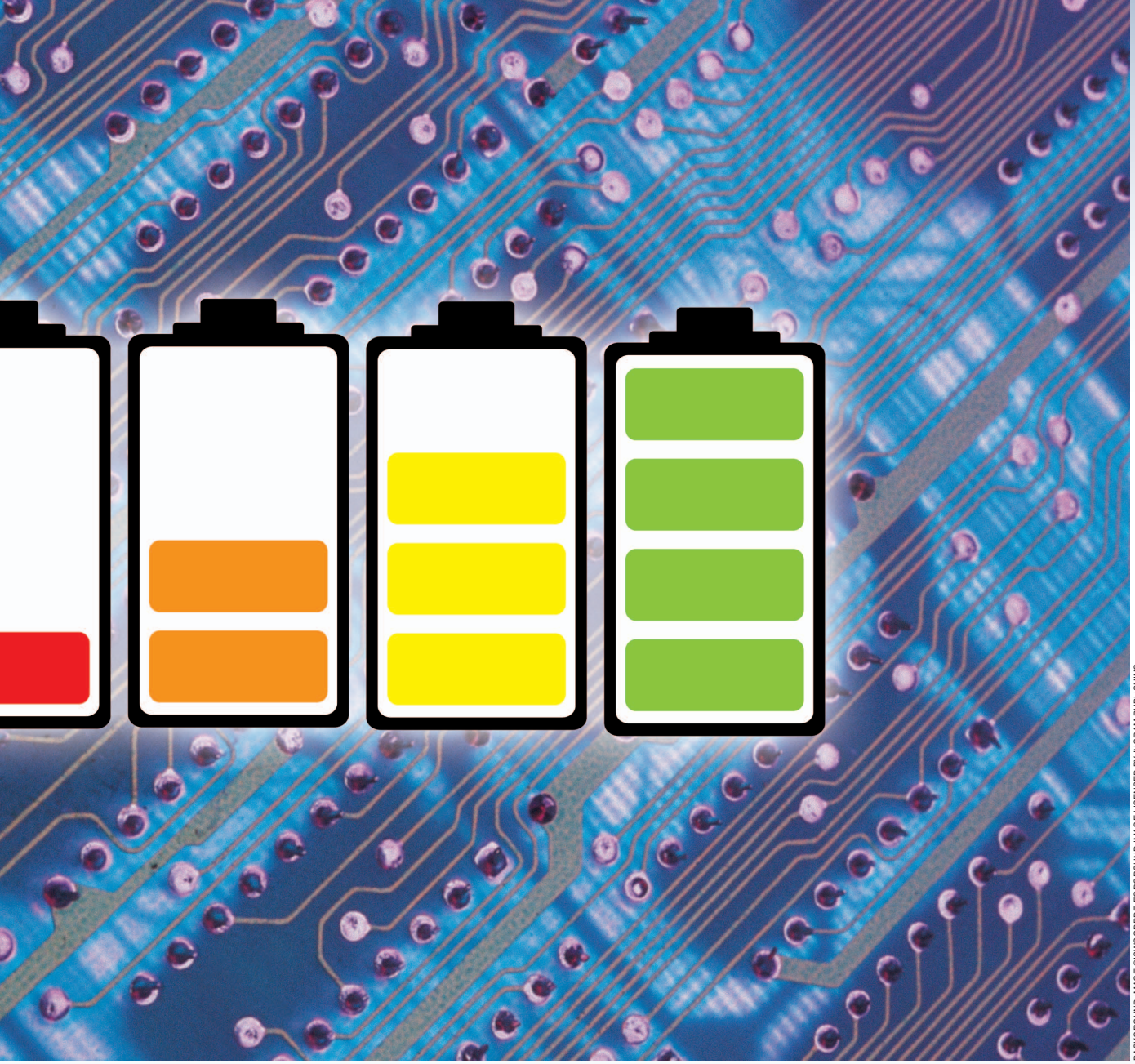
I. Introduction

With the surge of low power embedded systems in consumer and commercial use, there has been a similar boom in research directed towards improving the power efficiency for these systems. When considering devices designed for applications such as supply chain management and the Internet of Things (IoT), using wireless power transmission over traditional bandwidths has become an appealing prospect for reducing cost and the need for periodic maintenance. At mid-range distances in the tens of meters and legally permissible power levels, ultra-high frequency (UHF) power transmission may be a sufficient replacement for a battery or other external power source, allowing for periodic ultra-low-power (1–100 μW) data processing and signal interpretation without the need for



an internal power supply. Bypassing the need for chemical power sources or "active listening" for incoming signals, passive systems with wireless power converters are capable of functioning for many times the lifespans of their constantly-active counterparts.

However, the wireless embedded systems field is characterized by diversity in the application requirements and a corresponding diversity in design philosophy. The differences between applications preclude the concept of a "universal" approach to the design of low power receivers, and require that every circuit must be considered separately to retain the efficiency, range, and cost required by their application. Thus, the design of wireless harvesting units must be characterized through critical tradeoffs, which can then be used by the designer to create the optimal circuit for a given application.

This paper presents a survey of these tradeoffs for the technologies used in UHF band wireless power harvesting. Given that extensive surveys of comparative efficiencies [1] and networking protocols [2] already exist, our analysis will focus specifically on the varying circuit structures for LC matching, rectification, digital processing, and tradeoffs in modulation/demolation choices along with appropriate results indicating the benefits and drawbacks of published models, theorems, and implementations.

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Table 1.
Operational frequency range of solar panels.

Frequency	Band	Notes	λ
270 THz	IR	Infrared	1.1 μm
430 THz	Visible	Red	700 nm
...	Visible	...	...
790 THz	Visible	Violet	380 nm
1.6 PHz	UV	Ultraviolet	200 nm

The rest of this paper is organized as follows: Section II details and compares energy harvesting alternatives. Section III introduces the content of the survey with a summary of motivating applications for RF energy harvesting and the design tradeoffs for these applications. The background sections IV, V, and VI introduce important context for the transmission of wireless RF power and the evaluation metrics for doing so and a stage model of the RF power harvester/communications circuit. The analysis portion of the paper is contained in sections VII, VIII, IX, and X. These sections cover RF power harvester design tradeoffs for impedance matching, rectification and voltage multiplication, power management, and communications, respectively. Section XI compares these various tradeoffs for reference, and Section XII concludes our findings. Appendix A provides a glossary of the abbreviations used throughout the paper along with references to the corresponding section where they are described.

II. Energy Harvesting Alternatives

In this section, we provide a unified understanding of energy harvesting and list the available energy sources and their characteristics.

A. Unifying the Understanding of Energy Sources

In general, *energy* is transported through the ability of "matter" or "waves" to carry a *force* within a medium such as water, air, or a solid material such as a metal. In energy harvesting, the ultimate goal is to intercept this transported force and convert it to electrical energy. This is achieved by applying the transported force to a transducer (e.g., a wind turbine), that transfers the force into the electrons in a circuit (via increased potential energy), thereby facilitating an electric current.

Figure 1. Three different solar panels: 1.5 W, 10 W, and 30 W. A coin is placed on the panels to allow comparison of relative and absolute sizes.

Depending on "what" originates and transports the force and which medium is used during transportation, energy sources can be broken down into two primary categories:

Mechanical Waves: Imagine a wind starting at some point on earth. The source of this movement is some atmospheric event that *pushes* the air in a certain direction. Since the air is made mostly of N_2 and O_2 molecules, pushing one atom (e.g., "O" within the O_2 molecule) against another will repel the destination atom. This will transfer the momentum of one atom to the next one, thereby moving that atom (and its covalent-bonded neighbor atom, hence the entire O_2 molecule) in approximately the same direction. According to conservation of momentum [3], some energy loss is expected due to some heating on either atom and due the bounce-back of the initial atom, potentially hitting another atom somewhere else. The net effect is that, the air moves and the force is transported from one atom to another through the medium (i.e., the air).

An analogy is a billiard table in which an initial billiard ball is thrown against another. The force is transported from one billiard ball to another based on the law of conservation of momentum. The transportation of the force continues until the final billiard ball is intercepted by one of the holes on the table (i.e., *harvested*). The intercepted billiard ball carries a force that is proportional to the very first billiard ball. This type of a force-carrying mechanism through "atom-pushing waves" is termed *mechanical waves* or *compressional waves*. Wind energy, sound energy, and vibration energy are transported through mechanical waves. They are harvested by using wind turbines, microphones, and piezo crystals as transducers.

Electromagnetic Waves: Imagine a valence electron losing energy and moving from a higher-energy state to a lower-energy state at some point on earth. Where will the lost energy go? According to the conservation of energy [3], it will radiate as a photon at the frequency determined by

$$E = h\nu = \frac{hc}{\lambda} \tag{1}$$

where ν is the frequency at which the photon is oscillating, corresponding to the wavelength λ. h is the Planck constant and can be thought of as being the energy that the photon carries *per cycle of oscillation*. This photon can continue its travel indefinitely until it encounters an atom (more specifically, an electron) along its path. When it hits an electron, if the electron can absorb the energy that the photon is carrying according to Eq. 1, it

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will become more energetic and will move from valence band to conduction band. Therefore, the force that the photon carries is transferred to the electron, and the photon vanishes.

The type of waves created by photons is defined as *electromagnetic waves* for which the medium can be any solid, liquid, or gas. Solar energy and RF energy are transported through electromagnetic waves. The transducers that can turn these electromagnetic waves into energy are the photo-diodes in solar panels and inductors, respectively.

B. Wind, Sound, and Vibration Energy Harvesting

To harvest wind energy, an electric motor is used, that contains a magnetic rotor. This setup facilitates the conversion of the mechanical energy of the wind into the rotation of the motor, which induces an electromagnetic force (EMF) on the rotor. This EMF is the harvested energy in the form of an electrical current. Although small scale turbines are available for embedded circuits [4], that produce a power output in the mW range, this is much less common than the large wind turbines designed to produce power outputs in the kW range [5].

In theory, sound energy can be harvested by using a microphone, though this is not as common. Vibration energy harvesting, on the other hand, is a viable alternative to provide power for sensors in areas that have sufficient vibration activity. Examples include seismic activity areas, subways, cars, industrial machinery, and raindrops on tree leaves. Commonly used transducers include piezoelectric and magneto-strictive materials [6]. The amount of harvested power is expected to be in the multiple-100 μW range for this type of energy harvesting.

C. Solar Energy Harvesting

In solar energy harvesting, the source of the energy is the photons that the sun generates during the nuclear reactions inside the sun. These photons travel from the sun to the earth in the form of electromagnetic waves and are intercepted by solar panels that turn photons into electrical energy. Table 1 shows the frequency band of the photons that solar panels can harvest. In additions to the entire visible light spectrum, solar panels can harvest the photons in a small UV and IR band as well.

Solar panels are made out of photo-diodes that have an exposed junction for the photons to hit. When a photon hits an electron of the Si atom within the photo-diode, it can move a Si valance electron from valance to conduction and give it sufficient energy to cross the PN junction. Therefore, the energy that the photon carries is converted to electrical energy. Figure 1 shows three different solar panels that can harvest output power levels of 1.5 W, 10 W, and 30 W. Their sizes are 3.5" × 5", 9.5" × 13.5", and 14" × 26.5", respectively. Their total surface area is 0.011 m^2, 0.083 m^2, and 0.24 m^2. The power output per unit area of these solar panels can be calculated as 130–140 W/m^2.

D. RF Energy Harvesting

Radio frequency (RF) waves are electromagnetic waves that originate at a transmitter in the form of a photon that is oscillating within one of the pre-determined transmission frequency bands such as UHF, SHF, or VHF, etc. Note the difference between RF and solar harvesting: In RF harvesting, the source is an *intentional electromagnetic radiation by an electronic device*, rather than the *natural radiation by the sun*. The most important consequence of this fact is that, the electromagnetic properties of the RF radiation can be determined by the transmitter.

RF transmission frequencies (e.g., UHF ranging from 300 MHz to 3 GHz) are substantially lower than the frequency of the photons hitting solar panels (270 THz–1600 THz), translating to a 5–6 orders-of-magnitude lower energy-per-photon for RF harvesting as compared to solar, according to Eq. 1. This very fact drastically limits the applicability of the RF harvesting to extremely small embedded systems.

E. RF Energy Harvesting for Embedded Systems

The primary focus of this paper is RF energy harvesting for embedded systems. Comparing solar and RF harvesting, we notice that the harvested power levels are consistent with photon transmission frequency (i.e., 4–5 orders-of-magnitude lower for RF per m^2). Despite this seemingly big disadvantage of RF power levels, RF harvesting is still a very useful and practical alternative for the following reasons:

- Passive RF circuits can function at 2–100 μW due to the ability of the state-of-the-art VLSI technology to

incorporate non-trivial circuit functionality within such a power envelope.

- Since the goal of an embedded RF system is to provide a highly specific and limited set of tasks, Application Specific Integrated Circuits (ASICs) are designed for these specific tasks that could achieve orders-of-magnitude power advantages as compared to generic circuits.
- Since RF energy can travel within materials such as water, plastic, matte glass, paper, etc., RF embedded systems can be placed in areas where there is no solar power or "exposed" sensory outlet. In such scenarios, RF power harvesting might be the only alternative.
- Backscattering communication allows a passive RF circuit to communicate with the transmitter (i.e., the interrogator) using a " μW" power source, thereby eliminating the need for a "mW" power source within the embedded circuit that would be necessary for active RF communication [7].
- Directed communication using "light energy" is possible between a source and an embedded system by using a laser beam. The receiver can simply use solar panels to intercept and harvest this energy. In fact, the amount of energy a laser beam can transmit is substantially higher than that of an RF antenna. However, directed communication using light energy has very limited use due to the implied hazards on the eyes of humans and other animals. For directed (i.e., dedicated-source) communication, RF is the most widely-accepted alternative.

RF harvesting can be broken down into two major categories:

Ambient RF Energy Harvesting: Passive harvesting systems may take advantage of local ambient RF energy to charge much larger power storage systems over extended or indefinite periods of time [8]–[10]. This ambient energy may come in the form of Wi-Fi, TV, or military broadcasting [11], as well as directed energy transmission. A typical ambient RF harvesting circuit is expected to generate power levels in the 2 μW/cm^2 range [4]. Passive ambient harvesting requires no data processing, focusing solely on the reception and storage of ambient radio energy. Unfettered by the need for modulation or interpretive processing, ambient harvesting will have naturally improved efficiency across the range of input power, and can make use of more extreme design methodology in the later circuit stages.

As they are often solely responsible for sustaining power levels in isolated systems, ambient power harvesters cannot rely on periodic maintenance and may require extensive power buffering systems such as supercapacitors and microbatteries to sustain the circuit during periods of inactivity. This requirement is offset by a relatively stable source of power, since ambient RF power is usually supplied by a fixed source (or collection of sources) such as a transmission tower, power levels will not fluctuate over time to the same degree as commercial RFID handhelds. These circuits also benefit from an essentially infinite charging period, unlike communication-centric RFID applications that dictate a finite time period for circuit charging, and thus have more leeway in their selection of power buffering elements.

RF ambient harvesting is common for applications for which it is impractical or even impossible to change the node batteries, such as hazardous industrial maintenance or extreme environment monitoring. Since a node at the bottom of a hazardous gas can or a high altitude will be expected to function for long periods without maintenance, it is critical to design circuits that are reliable while still taking maximum possible advantage of available ambient power. Thus, ambient harvesters tend to have extended antennas and impedance networks but relatively few rectifier stages, and are followed by extensive buffering systems to preserve power for periods of high processing activity or low ambient exposure.

Dedicated-Source RF Energy Harvesting: A dedicated-source RF harvesting circuit at a short range is expected to generate power levels in the 50 μW/cm^2 range [4]. An example is an RFID chip that is powered by an RFID interrogator [12].

In this paper, we focus on dedicated-source RF energy harvesting, which enables embedded devices not only to recharge batteries but also supports communication and wake-up functions, as will be described in the following section.

Figure 2. A passive RFID tag (left) used in a retail store to protect against theft, and an active RFID tag (right) that is attached to the window of a car, used in New York State E-ZPass toll booths.

III. Motivating RF Applications

Radio frequency power harvesting refers to the harvesting of the energy in a wireless signal through an antenna to power an embedded device. While the technology used to achieve this has certain universal similarities, the applications for wireless power harvesting are extremely diverse,

and may affect the design philosophy of the different elements within the circuit. Optimizations for one application may be detrimental to another, sacrificing range for efficiency, size for durability, or complexity for cost in ways suited only to a specific task. Thus, the needs of the application must be fully established before any design decisions take place, and be repeatedly reconsidered to make sure circuit tradeoffs are given proper weight in the final product. The following section provides three broad families of power harvesting applications to provide context for the surrounding research, along with brief technical descriptions of the design tradeoffs for each, which will be fully elaborated upon in later sections.

A. Radio Frequency Identification (RFID)

RFID remains the most common and ubiquitous use of power harvesting technology. RFID has been widely accepted as the technological standard for supply chain management and industrial data tracking, and will undoubtedly see further expansion as the easily integrated transceiver chips (referred to as "tags") are adapted to smaller sizes and costs. For example, medical data acquisition is an emerging field that can significantly benefit from RFID [13]. *Passive* RFID design, which centers exclusively around wireless power harvesting, has a number of advantages over *active* design with traditional power sources [14], [15]. An example of each type of tag is shown in Fig. 2. Passive tags have extended lifetimes, do not require periodic maintenance, and can be fabricated at smaller size and cost than their battery powered counterparts. However, without the advantage of external power, passive tags must overcome a number of technical challenges to meet competitive range and performance requirements.

RFID is characterized by two way communication - the transceiver must not only receive data, but also transmit it via reflective backscatter managed by an internal oscillator and signal modulator. In addition, RFID chips must be extremely small and inexpensive to be commercially competitive, and are almost always implemented on a single integrated IC with an extremely small physical footprint. While these design parameters restrict the tools available to IC engineers, the massive scale on which RFID chips are produced invariably means that high precision technology is available; thus, parasitic effects can typically be predicted with higher precision than other technologies, and accounted for via simulation and optimized design models.

RFID functionality is highly limited, since their sub-$100\,\mu$W power budget prohibits the implementation of elaborate on-chip computations (e.g., strong encryption [16]). RFID is most frequently used in supply chain tracking, personnel monitoring, and other commercial systems that typically require some onboard processing for every query. This places a great deal of design emphasis on improving efficiency while reducing size and cost. Additionally, the need for two-way communication requires additional consideration for the modulation component, which sacrifices some power efficiency in order to communicate back to the source. Thus, RFID chips tend to have lower numbers of rectifier stages for efficiency, small and inefficient antennas, more complex impedance matching networks to provide backscatter, little to no power buffering to conserve space, and minimal computing power.

B. Wireless Sensor Networks and Wake Up Radios

A relatively recent application for RF power harvesting is the enhancement and control of Wireless Sensor Networks, or WSNs [17]. These networks are defined as collections of autonomous systems to monitor environmental conditions, and may be used for research, industrial oversight, or biomedical applications. Unlike RFID, WSN nodes are responsible for more activity than the simple storage and transmission of data, and thus usually necessitate an onboard battery to power the relatively energy-intensive tasks of sensing and processing data (e.g., temperature, vibrational, or chemical monitoring). However, passive power harvesting systems may assist WSN nodes in a number of ways in conjunction with this primary power source [18]. Though their harvested power may not be sufficient to charge the larger scale energy storage, a passive chip may be used as a Wake Up Radio (WUR) that generates a wake up pulse upon receiving a command from a nearby transmitter [19]–[21]. Use of a fully passive WUR means that the active portion of the chip will only be active for short periods, and does not need to actively listen for commands during downtime. Designing the chip to be entirely power inert when not being queried for data can drastically improve chip lifetime, allowing systems that would otherwise require regular battery maintenance to expand to lifetimes of several years.

Wake Up Radios often do not require backwards communication, since their only purpose is to interpret a command and perform simple actions (e.g., waking up the main sensor system). Thus, they may take advantage of certain efficiency approaches that cannot be exploited by conventional RFID tags, by omitting efficiency-impeding elements such as modulators and digital processing, in favor of a simple correlator and pulse generator to wake the deactivated sensor system. This improvement in efficiency and lack of a backscatter system may lead to improvements in both range and operating time over default tags.

The specific applications for WSN networks thus tend to favor open environment monitoring, animal research, and isolated robotic systems. Thus, these designs tend to emphasize extreme range, but need very little power to perform their single wakeup operation and often have insignificant

Table 2.
Commonly used Radio frequencies (RF) and corresponding wavelengths. $\lambda/2\pi$ indicates the end of the inductive near field region. $\lambda/4$ plays an important role in RFID antenna design.

Frequency	Band	Notes	λ	$\lambda/2\pi$	$\lambda/4$
125–134 KHz	LF	unregulated	2.3 km	367 m	577 m
13.56 MHz	HF	ISM global	22 m	3.5 m	5.5 m
865–868 MHz	UHF	EU: ISM	35 cm	5.5 cm	8.7 cm
902–928 MHz	UHF	USA: ISM	33 cm	5.2 cm	7.2 cm
2.4–2.48 GHz	UHF	ISM	12 cm	2 cm	3 cm
5.8 GHz	SHF	ISM	5.1 cm	0.8 cm	1.3 cm
5.8 GHz	SHF	ISM	5.1 cm	0.8 cm	1.3 cm

limitations on size and cost. WSNs tend to consist of large and efficient antenna/impedance matching networks, followed by many rectifier stages to improve sensitivity, and very few buffering and computing elements in the back end.

IV. Background: Transmission Restrictions

Before approaching the individual sections of the RF power harvesting circuit in full detail, it is useful to define several operational metrics and legal limitations that will be continually referred to throughout this paper. In this section, the legal and logistical restrictions on frequency and power are defined and discussed.

A. Transmission Range: r

The wavelength (λ) of an Electromagnetic (EM) wave radiated from an RF source at frequency f is

$$\lambda = \frac{c}{f} \Rightarrow \begin{cases} r \le \frac{\lambda}{2\pi} & \text{Near Field Inductive} \\ s\frac{\lambda}{2\pi} > r \le 2\lambda & \text{Near Field Radiative} \\ r > 2\lambda & \text{Far Field Radiative} \end{cases} \quad (2)$$

Figure 3. A P_{EIRP}=1 W, 915 MHz RFID reader/interrogator.

where c is the speed of light and r is the distance between the RF source (transmitter) and the RF receiver (e.g., RFID tag antenna). The significance of the $\lambda/2\pi$ metric is that, this is the distance below which an RF transmitter and an RF receiver can establish an *inductive coupling*, similar to the coupling between the two ends of a transformer. Above $\lambda/2\pi$, communication is by means of *radiative coupling* [22].

While Eq. 2 ignores the size of the radiating antenna, these boundaries are typically placed at

$$\frac{\lambda}{10} < D < \frac{\lambda}{2} \begin{cases} r \le 0.62\sqrt{\frac{D^3}{\lambda}} & \text{NF Inductive} \\ 0.62\sqrt{\frac{D^3}{\lambda}} > r \le \frac{2D^2}{\lambda} & \text{NF Radiative} \\ r \gg \lambda, r \gg D & \text{FF Radiative} \end{cases} \quad (3)$$

when the radiating antenna size, D, is taken into account [23], which can be simplified to Eq. 2 since optimum antenna sizes are proportional to λ. Up to $r \le 2\lambda$, the communication between the RF source and the receiver is subject to strongly-interacting diffraction patterns, and is called *near field communication*. $r > 2\lambda$ is the *far field communication* region which is strictly radiative and the propogating waves behave like plane waves. These two types of communications have a dramatic affect on the way RFID tags are designed: In the near field inductive region, the power decay is proportional to $1/r^3$, whereas, in the far field region, it is proportional to $1/r^2$. Table 2 shows commonly used RFID frequencies, their corresponding wavelengths (λ) and the end of their inductive near field distance ($\lambda/2\pi$). The last column shows the $\lambda/4$ value which will play an important role when designing RFID tag antennas as will be discussed in Section VII-F.

B. RF Operational Frequency

RF power harvesting is possible at a large range of frequencies, from near-field inductive coupling at only a few KHz to satellite power transmission at ≥30 GHz. However, the RFID standard and most significant breadth of research has centered around the UHF band (300 MHz–3 GHz range in Table 2). UHF band frequencies, which are also widely used by cellphones and mobile devices, are convenient for use in everyday spaces due to their balance between flexible range and low interference with environmental objects. However, the characteristics of the wave still vary significantly within the UHF range depending upon the wavelength parameter λ, which dictates antenna size, environmental attenuation, and

receiver component choice. Lower frequencies require larger antennas, attenuate less with environmental conductors, and require less precise circuit components for impedance matching; conversely, higher frequencies can utilize very small antennas, but attenuate heavily with range and are so sensitive to parasitics that they may only be feasible for Integrated Circuitry (IC). This tradeoff, along with its implications, is further discussed in Section VII.

The 125–134 KHz range shown in Table 2 found great use in *wireless charging*. The *Qi* standard [24], [25] introduced by the Wireless Power Consortium [26] is now implemented as an emerging means for wirelessly charging consumer devices such as laptops and cellphones, though, typically in the 110–205 KHz range [27]. 13.56 MHz, used in smart cards [15], [28], received great attention in early RFID research [14], [29]. These bands have a very large λ value and are best used for *inductive coupling* or *magnetic resonance*, rather than *EM wave propagation* or *radiative coupling*, which is dominant in the ISM frequencies. Inductive coupling can be an efficient method of power transfer at distances less than 1 m, but attenuates quickly at greater ranges, and additionally requires much larger antenna sizes and an altered circuit design to suit magnetic coupling. For these reasons, it cannot be used for far-field power harvesting, and is regarded as outside the scope of this paper.

In this paper, we focus on the most common 915 MHz and 2.4 GHz bands used in RFID and similar technologies, which are specified as open bands (called the *Industrial-Scientific-Medical* or *ISM bands*) within the United States and present opportunities for both directed and ambient power harvesting. 915 MHz is an easily accessible band with reasonable range and easily-fabricated reception circuitry, whereas 2.4 GHz may achieve greater ranges and smaller antenna sizes at the cost of more expensive impedance matching components and greater environmental attenuation. Other frequencies may theoretically be used, but may be limited by commercial ownership or strict regulation of legally transmittable power, and thus have less representation in academic literature.

C. Antenna Transmission Power

For any wireless harvester device, energy must be gathered from the transmissions of one or more transceiver nodes that radiate RF power. The legal level of power output for these nodes, be they commercial transmission towers or simple consumer transmitters, is strictly regulated in most countries. The US limitation on maximum *Equivalent Isotropically Radiated Power* (EIRP) is 4 W, which applies to both the 915 MHz and 2.4 GHz bands of interest. EIRP is directivity independent, meaning that transmitted power cannot be increased with a narrower beamwidth - thus, any gains in power reception may only be achieved through antenna gain or range restriction. Figure 3 shows an Impinj Speedway IPJ-R1000 RFID reader/interrogator, which has a P_{EIRP}=1 W transmission power, operating at 915 MHz [12].

As several of the critical tradeoffs in a power harvesting system are range related, it is useful to estimate the power that will be available to a receiver node by distance. Several methods exist for predicting the power received by an antenna at a given range. The most commonly used equation is the *Friis Transmission equation*, developed by Harald T. Friis in 1945 to calculate the power transmitted between two antennas in theoretical free space as follows:

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi r)^2} \tag{4}$$

where P_t is the non isotropic transmission power, P_r is the incident power at the receiving antenna, and G_t and G_r are the gains of the transmitting and receiving antenna, respectively. $\lambda^2/(4\pi r)^2$ is the free space loss factor.

This model can provide a useful upper limit for the maximum possible range available for a given transmitted power and antenna aperture. However, note that this equation assumes ideal free space, without any form of environmental attenuation - most real-world measurements will experience higher order distance attenuation, $1/r^3$ or even $1/r^4$, causing far lower power levels in typical urban spaces. For predictions intended to account for these real world influences, a statistical log-shadow methodology may need to be used to determine a range of expected power values. Together, the EIRP and Friis Power define two important upper limits for every wireless harvester design, which can be used to determine early feasibility goals and estimates. Available power

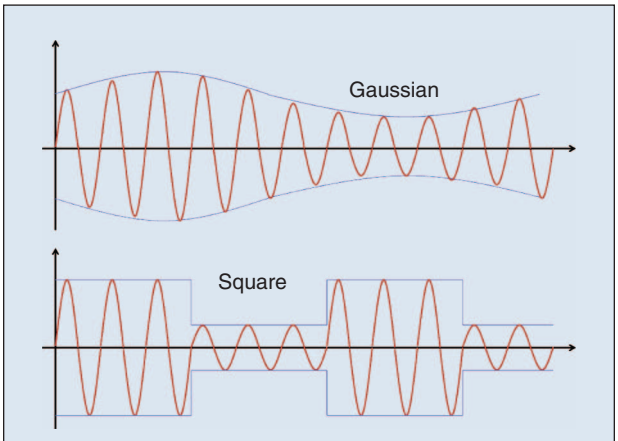


Figure 4. Gaussian and Square Power Optimized Waveforms (POWs).

at the antenna can never exceed the EIRP, regardless of range, and when evaluated at a distance will almost always fall below the Friis available power density, except for certain highly reflective environments. However, a few methods exist for attempting to boost instantaneous power while retaining the same average power, which are discussed further in Section IV-D.

D. Transmission Improvements

For any RF signal to be received and harvested for power, it must first be sent by a transmitter. This may take the form of a single dedicated node, or as network of coordinated nodes, or even as ambient noise from a broadly modeled collection of sources. For RFID, single dedicated nodes, called RFID Readers, are the most common; alternatively, ambient power harvesters almost never have a single source and may receive from distant transmission towers and nearby mobile devices simultaneously. It is important to note that readers designed to actively interpret backscatter communication as well as transmit power tend to be quite sensitive and have vastly higher power and size traits than embedded tags, and thus have dramatically different design paths that do not adhere to any of the tradeoffs listed for receiver end technology. For this reason, hardware and networking protocols for transmitter systems are not included within the scope of this paper. However, the transmitted signal and its quality of reception may be improved through the use of specially optimized waveforms, careful antenna design, and improved decoding methods.

Power Optimized Waveforms (POWs): Carefully designed waveforms optimized to provide higher peak voltages can substantially increase the overall efficiency of the harvester system, and are implemented entirely on the transmitter end, requiring no changes to the receiver architecture. POWs utilize periodic amplitude fluctuation to maximize the voltage at the input of the RFID receiver, thereby increasing its efficiency [30]. Since the average RMS power remains the same, POWs can be used to improve voltage-related performance without violating the power transmission limits present in most countries, and provide a means of overcoming rectifier voltage thresholds without the necessity of a system power increase. POWs can thus be used to increase both input sensitivity and efficiency of the receiver, with few tradeoffs in receiver architecture [31]. Several potential POW shapes exist, as outlined in [32]–[34], varying from Gaussian waveforms to simple square waves as shown in Fig. 21 that simply duty cycle the signal to achieve a higher voltage amplitude at the same RMS power. As will be described in Section VI, the *voltage* at the RF receiver input will play a crucial role in the efficiency of an RFID receiver.

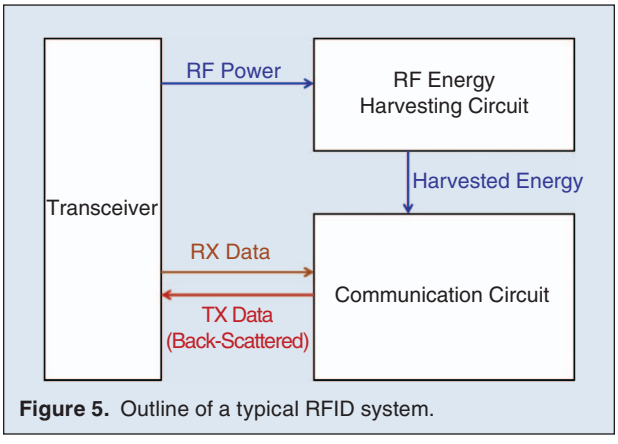


Figure 5. Outline of a typical RFID system.

The advantages of each waveform vary from application to application, and are often dictated by the data rate and desired bandwidth of the signal [34]. Due to their irregular signal, POWs may cause higher voltage rippling at the receiver, which must be smoothed with buffering systems before being passed to the IC. Additionally, in cases where backscattering communication is necessary, POWs may impose limitations on the types of modulation available and the error rate of these communications. A detailed description of modulation types will be provided in Section X-D. Circuits intended only for power harvesting do not suffer from these limitations, as they do not require demodulation or high bitrate protocols. Such systems may even use entirely chaotic waveforms to increase efficiency [35]. However, since many harvester-only systems are intended for ambient harvesting from commercial radio towers or other wide-dispersal sources, they do not have the luxury of a programmable transmitter and are thus unable to harness the advantages of POWs. Further potential applications of POWs are discussed in Section IX-C.

Signal Encoding: Passive harvesting systems depend upon the amplitude of the incoming signal for power, and thus many systems will benefit from the use of specialized encoding types such as Manchester encoding, where the DC value of the signal is independent of the data sent. Using these forms of encoding ensures a consistent average power entering the system, and ensures that data with a low overall duty cycle will not inadvertently starve the system of power. However, these more advanced encoding schemes may come at the expense of increased bandwidth and more complex demodulation circuitry. These tradeoffs should be carefully considered before deciding upon an encoding type that services both power supply and bandwidth/complexity constraints without debilitating the performance of either.

Antenna Optimization: The design of RFID antennas is a field of its own [36], [37], with a wide range of variables impacting the performance, size and cost of antenna

implementations [38]–[40]. Many antennas intended for commercial use are designed using evolutionary algorithms to reach optimal power transfer for a given size [41]. Others, especially those used for research applications, may be printed inexpensively with a PCB prototyping process, and dynamically modified when optimizing the performance of the circuit front-end [42]. The traits of these antennas are highly application-specific, and are dictated by pre-existing requirements for cost, size, and manufacturing quality.

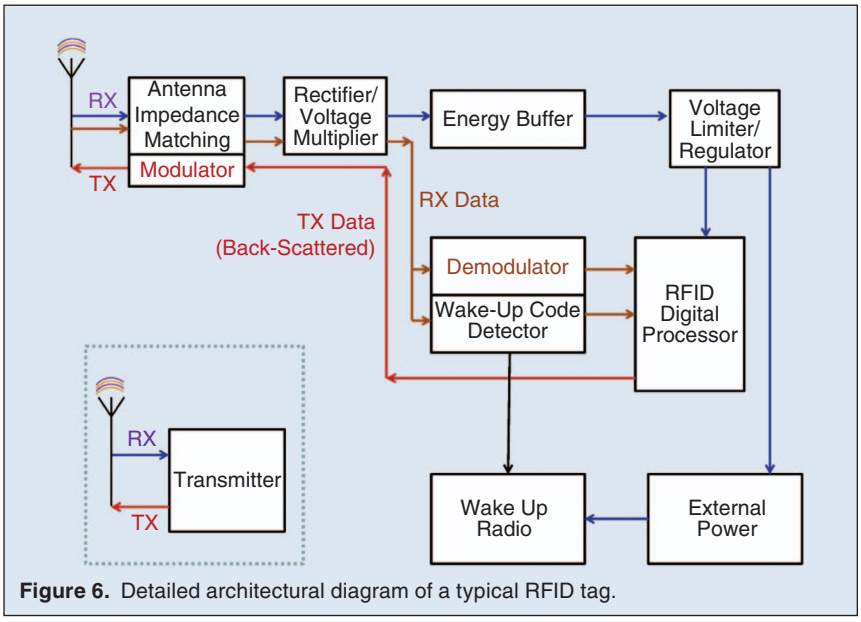


Figure 6. Detailed architectural diagram of a typical RFID tag.

However, since all common antennas can be characterized by a set of ideal and non-ideal parameters, only a few aspects of antenna design factor into the discussion of power harvesting efficiency. Most antennas are designed to minimize all reactive elements and assume a single real value for input impedance, usually 50Ω, 75Ω, or 300Ω for commercial antennas, or a wide range of values for custom ones [43]. As larger resistance values result in higher harvested voltages as we will discuss in Section VIII, maximizing this value will lead to efficiency gains, though this may be difficult for electrically small antennas (ESAs) [44] or those with limited manufacturing detail [45]. It may also be assumed that at the high frequencies of UHF, some reactive components will exist as parasitics, and will have a non-ideal effect on the performance of the circuit. However these parasitics can be accounted for during the impedance matching process, and the voltage at the antenna may be improved through LC resonance boosting if certain conditions are met, a process that is further discussed in Section VII.

V. Background: Building Blocks

The general outline of an RFID system is shown in Fig. 5, consisting of a transceiver, harvester, and a communicator. The antenna assumes the *transceiver* role since it not only receives RF power and data, but also backscatters a portion of this power to be able to communicate back to the transmitter. *RF power harvester* is the portion of the circuit responsible for extracting the available power at the antenna efficiently and delivering it to the digital portion of the IC. *Communication* portion of the IC is responsible for demodulating incoming data and modulating outgoing data via backscattering, to establish a communication link with the source.

To accomplish these three tasks, RFID systems consist of several distinct circuit stages shown in Fig. 6. While these stages can be individually characterized and have distinct roles within the circuit, each stage can dramatically impact the comparative performance of the others and the efficiency of the overall circuit. To successfully apply Figure of Merits (FoMs) to the design of an RFID system, it is critical to use consistent models and methodology, as an isolated approach may only improve a single metric and degrade others. To promote a global design approach and consistent treatment of the tradeoffs, the Analysis portion of this paper will be dedicated to illustrating each stage in detail and describing their effects on the system as a whole. The remainder of this section illustrates a roadmap of these stages.

Transmitter: While it is usually considered separately from the power harvester design, the efficiency of any power harvester system begins at the *transmitter*, which broadcasts the electromagnetic signal under the constraints of legal regulations and the physical transmission properties of the environment. While improvements in transmitter hardware and functionality will have no bearing on the power harvester efficiency, changes to the waveform of the transmitted wave may increase rectification efficiency by increasing the peak antenna voltage (consecutively, peak rectifier input voltage) as discussed in Section IV-D. The waveform of the transmitter may also be responsible for carrying information, both as instructions sent to the receiver, and as a carrier for backscattered communication being returned to the transmitter through impedance mismatch. These two communication signals may affect the efficiency of the power harvester through their duty cycle, as the power can fluctuate between high and low bits for certain forms of keying. However, this effect may be remedied through certain types of data encoding.

Antenna Impedance Matching: The first element of the power harvester itself is always the *antenna*, which creates a usable electronic waveform from the local RF power. An essential factor for any RF application is proper impedance matching to the antenna, since without a *passive LC network*, much of the power received at the antenna will be reflected back into free space. The specifics of this matching process vary based on the antenna size and construction, and also upon the passive methodology of the receiving circuit input. In many cases, changes in impedance reflection are also utilized by active circuit components to achieve the backscatter communication described earlier. The technological precision of this stage is often the most critical in the entire circuit, as even small changes in the resistive or reactive elements of the matching network impedance can cause disproportionately detrimental effects on the efficiency of the antenna reception. As an added complication, the matching network and incoming waveform may be utilized in some technologies to boost the signal's voltage amplitude using resonant amplification, raising the rectifier peak input voltage and thus the efficiency of the rectifier as well as the matching network.

Rectifier/Voltage Multiplier: Unfortunately, the voltages achievable via LC amplification alone are still typically insufficient to run a digital IC at the output of the power harvester system. Once the signal has been received by the antenna and amplified by the LC matching component, it must be passed through a *voltage multiplier* to reach a level usable by digital circuitry. Voltage multipliers often consist of several full wave rectifiers connected in cascade, which simultaneously rectify the sinusoidal AC waveform to DC and multiply it to a higher voltage. Due to the operating voltage drop over the diode or MOS components of the rectifier stages, the peak voltage at the input rectifier terminals is critical to the efficiency of the overall multiplier, and thus even small levels of voltage boosting in the LC stage can drastically improve the performance of this unit. Additionally, care must be taken that the number of cascaded multiplier stages is at the optimum point, as too few stages will result in an insufficient voltage output and sensitivity, while too many will generate harmful parasitic capacitance that will detrimentally affect the preceding antenna matching process.

Energy Buffer, Voltage Regulator: After the final stage of the multiplier, the DC output is typically passed into an *energy buffer* to remove ripple and provide consistent power availability. This buffer may be as small as a capacitor of several nanofarads, or as large as a digitally-controlled supercapacitor or rechargeable microbattery. The nature of the buffer element is dependent upon the application; many power harvesting applications do not even consider the final capacitor to be a buffer, but simply another stage element of the multiplier topology. In other cases, a large and intelligently controlled power buffer is critical to the function of the circuit, and allows for substantial gains in range and operating time that could not otherwise have been attained. Performance of this stage is typically tied to the operation of the circuit's *voltage limiter* or *regulator*, and circuits with a sophisticated back-end may integrate these two systems together to improve power efficiency, decrease losses, and provide dynamic resistive matching to the antenna.

RFID Digital Processor: Finally, after being fully processed, the signal can be used to power the *digital back-end*. This back-end is often the most heavily engineered element of the entire harvester, but is also the most application specific, and is difficult to generally categorize due to no specific digital element being present in every power harvesting circuit. The circuit can include any number of components, so long as they fall under the voltage and current consumption limits of the multiplier input and buffer element. Some ambient circuits may contain only as much circuitry as they need to manage the power buffer and regulator, utilizing a wake-able active component to perform processing operations as it becomes necessary. Other chips, such as RFID commercial trackers, may contain a detection-focused digital communications unit with oscillators, backscatter modulation, and nonvolatile memory. These elements may dynamically alter the structure of preceding units by altering the connections of the LC network, multiplier, and regulator to perform backscattering and reactive antenna calibration.

Modulator, Demodulator, Wake-Up Code Detector: The communication portion of a typical RFID circuit includes a demodulator that extracts the data being transmitted by the transmitter, as well as a backscattering modulator that modulates the load of the antenna to intentionally cause mismatches with the intention to transmit back data. A dedicated Wake-Up code detector can be incorporated into the RF circuit to detect an ID from the transmitted signal, which is used to wake up an active unit, such as a wireless sensor node.

Historically, the most common implementation of this series model of the wireless power harvester is a simple LC impedance matching front-end, a diode or transistor based Dickson-style multiplier, and a non-buffering limiter before the digital IC. These stages optimize power transfer from the antenna, boost the voltage to a suitable level for digital circuits, and prevent circuit damage from voltage overload, respectively. However, many publications have sought to improve upon this standard by altering one or more stages, by altering structure, changing process technology, or utilizing more specialized

mathematical models. To provide a full and accurate summary, each stage of the model presented above will be addressed independently across the following Analysis portion of this survey.

VI. Background: Evaluation Metrics

As discussed in the introductory sections, the wide span of applications in which wireless power harvesting may be used means that no single Figure of Merit (FoM) may be used to evaluate the quality of a design. However, it is useful to define the efficiency, sensitivity, peak voltage and output voltage as the performance-critical evaluation metrics. These central FoMs determine the ability of the circuit to receive power at a distance and convert it efficiently, and while improving them may not always be the goal of a circuit designer, it is always critical that some standard of performance be met for the circuit to function competitively. Most of the critical tradeoffs in a power harvester circuit are between one of these metrics and the auxiliary metrics of low cost, low size, ease of manufacture, and high reliability. These main FoMs are defined as follows:

A. Power Conversion Efficiency (PCE)

A widely used evaluation metric, Power Conversion Efficiency (PCE), refers to the proportion of the power received at the antenna that is successfully relayed through the harvester rectification circuitry and applied to the *load*. Here, we use the term *load* to refer to the parts of the circuit that need a steady DC voltage to operate, such as the communication circuitry, processing circuitry, sensing circuitry (if any) and more. With a slight abuse of terminology, we will use the term Integrated Circuit (IC) and load interchangeably, e.g., *load current* vs. *IC current*. A high PCE percentage indicates an efficient rectifier circuit, but power losses due to nonlinear component thresholds, leakage currents, and parasitics always exist in a practical circuit. PCE is defined [46]–[48] as the relationship between the *absorbed power* and the *load power* as shown in Eq. 5, and does not take signal reflection at the antenna into consideration.

$$\text{PCE} = \eta_c = \frac{P_{\text{load}}}{P_{\text{absorbed}}} = \frac{P_{\text{load}}}{P_{\text{incident}} - P_{\text{reflected}}} \tag{5}$$

B. Sensitivity (P_{dBm})

The minimum power required for the IC of the receiving device to perform its intended task is defined as its Sensitivity. While less obvious than the blunt usefulness of PCE for evaluating circuit quality, sensitivity is often a more critical metric for evaluating the application of embedded systems, as minimum power is what dictates the range, buffering requirements, and computing capacity of a device.

While maximizing sensitivity and efficiency are not mutually exclusive goals, their relationship may be complicated by the fact that PCE is often dependent upon input power. Operating at the absolute minimum possible input power usually results in a lowered PCE, since conversion efficiency tends to increase with input power and voltage amplitude. Additionally, designing circuits with technology such as zero threshold CMOS may increase sensitivity, but the leakage currents inherent to these processes may impair the circuit efficiency to unacceptable levels. A circuit seeking to competitively assert itself in the commercial market will have to balance between these two metrics, typically dictated by the application assigned to the IC and the ideal range at which the circuit should perform. Sensitivity is measured in DeciBel-milliWatts (dBm) according to the formula below:

$$\text{Sensitivity} = P_{dBm} = 10\log_{10}(P_{mW}) \tag{6}$$

where P_{dBm} and P_{mW} are the power values expressed in terms of Decibel-milliWatts and milliWatts, respectively. As an example, most competitive far-field RFID circuits have a sensitivity between –25 dBm and –10 dBm, corresponding to operating input power levels between $3\,\mu$W and $100\,\mu$W.

C. Peak Passive Voltage (V_{peak})

The efficiency and sensitivity of a standard power harvester circuit are highly proportional to the amplitude of the sinusoid between the LC matching network and the rectifying stage ladder. This relationship, unique to wireless power harvesting, is commonly referenced in the literature but never given a specific emphasis. For the purposes of simplicity, this paper will define the *Peak Passive Voltage* (V_{peak}) as the peak amplitude of the voltage sinusoid observed at the output of the antenna impedance matching network (i.e., input terminals of the rectifier/voltage multiplier).

V_{peak} defines the sensitivity and efficiency of the rectifier via its relationship to the voltage threshold V_{TH} at the rectifier input terminal. As the V_{peak} rises above V_{TH}, the PCE will increase, but allowing the V_{peak} to drop below V_{TH} will deactivate the multiplier, defining the sensitivity. V_{peak} is also related to the rectifier output voltage, as the rectifier ladder will output a voltage multiple of the V_{peak} depending upon the number of stages.

D. Rectifier Output Voltage (V_{out})

The DC voltage amplitude at the output stage of the rectifier/voltage multiplier is defined as the Output Voltage and is usually recorded at the absolute worst case scenario

(i.e., minimum input power conditions). In general, output voltage is seen as a technological requirement rather than a metric to optimize, since the operating voltage of most IC technologies cannot be further improved without significant power losses or increases in cost, and thus this performance measure can only dictate the number of stages in the voltage multiplier.

E. Regulator Dropout Voltage (V_{dropout})

The responsibility of the voltage limiter/regulator is to reduce V_{out} down to V_{DD} and regulate it at this stable DC value. Since the regulator will require a voltage difference between its input and output (referred to as "dropout", V_{dropout} in the literature), $V_{\text{out}} > V_{\text{DD}}$ must hold for good regulation. The regulation is achieved according to

$$\text{Regulator Dropout Voltage} = V_{\text{dropout}} = V_{\text{out}} - V_{\text{DD}} \tag{7}$$

F. Load Voltage (V_{DD}) *and Load Current* (I_{DD})

The entire digital portion of the RF circuit is typically fed from a stable DC voltage, V_{DD}. The current draw from V_{DD} by the digital back-end (the load) is referred to as I_{DD}. As most IC technologies require voltages of over $V_{\text{DD}} > 1\,\text{V}$ to function properly, V_{DD} is often the dominating parameter for sensitivity, since it is assumed that any lower values of input power will result in an insufficient voltage to power the digital section of the IC. Voltage values above acceptable levels are managed by a limiter or a regulator, preventing damage to sensitive IC components.

G. Overall System Efficiency (η_o)

For cases where the entire circuit needs to be collectively examined for efficiency, rather than just comparing rectifier performance, the overall efficiency, η_o, can be examined using Eq. 8 based on the incident power [46], and thus overall power efficiency will include efficiency losses from impedance mismatch and reflective scattering at the antenna level.

$$\text{Overall System PCE} = \eta_o = \frac{P_{\text{load}}}{P_{\text{incident}}} \tag{8}$$

Since η_o is heavily dependent on the antenna and circuit process precision for the passive components, it may vary significantly between different implementations of the same circuit design, and is less commonly included in RFID literature as a performance metric. Implementations of LC matching circuits are often intentionally excluded through the use of a hard-wired RF signal generator for testing, or are mathematically described as having abstracted efficiency boosting traits, leaving any numerical record of efficiency to the manufacturer once the full benefits of manufacturing scale have been applied. For the purpose of comparing publications within this survey, studies that have examined the overall efficiency rather than the conversion efficiency will be clearly indicated to prevent confusion.

Eq. 8 incorporates efficiency losses due to the three distinct stages that the incident antenna power must transfer through to turn into a stable load power @ $V_{\text{DD}} \times I_{\text{DD}}$. The antenna and the impedance matching network efficiency is the ratio of the incident antenna power and the power delivered into the rectifier input as follows:

$$\text{Antenna/LC Nwk Efficiency} = \eta_{\text{ant}} = \frac{V_{\text{rect}} \times I_{\text{rect}}}{P_{\text{incident}}} \tag{9}$$

where V_{rect} and I_{rect} are the RMS voltage and current at the input of the rectifier. Note that, η_{ant} includes the power loss due to the need to communicate via backscattering. The rectifier efficiency is the ratio of the incoming rectifier power and the DC power output from the rectifier into the regulator and can be defined as:

$$\text{Rectifier Efficiency} = \eta_{\text{rect}} \approx \frac{V_{\text{out}} \times I_{\text{DD}}}{V_{\text{rect}} \times I_{\text{rect}}} \tag{10}$$

where I_{DD} is the load current, which is approximately equal at both the input and the output of the regulator, and V_{out} is the output voltage of the rectifier. The regulator efficiency is dominated by the required minimum dropout voltage and is defined as η_{reg} as follows

$$\text{Regulator Efficiency} = \eta_{\text{reg}} \approx 1 - \frac{V_{\text{dropout}}}{V_{\text{out}}} \tag{11}$$

which is typically less than Eq. 7 due to the quiescent current sources required to operate the regulator, hence our $\approx$ notation. Combining Eq. 9, Eq. 10, and Eq. 11, we arrive at Eq. 8, which can be rewritten as

$$\eta_o = \frac{P_{\text{load}}}{P_{\text{incident}}} = \eta_{\text{ant}} \times \eta_{\text{rect}} \times \eta_{\text{reg}} \tag{12}$$

where η_{ant}, η_{rect}, and η_{reg} are the individual efficiency of the antenna and the LC matching network including reflective power losses at the antenna, the rectifier ladder, and the voltage limiter/regulator, respectively.

H. Auxiliary Metrics

Other metrics also affect the circuit design philosophy. *Cost per unit* is defined as the monetary expense of manufacturing an individual design, a critical value for circuits in commercial products and other high volume applications. Cost is generally related to *ease of manufacture*, which will degrade with unusual technologies - much of the literature in the 2000–2010 era has focused on converting from the efficient but difficult to manufacture Schottky diodes to the more universal CMOS technology. *Physical size* may also be an important merit for commercial and

research applications, which can exclude large antennas or high-area LC matching networks from use in the design. *Reliability* may be a concern for ICs with an unusually long expected lifetime or stressful environment, which may necessitate larger circuits, PCE-lowering compensation overhead, and redundant circuit elements.

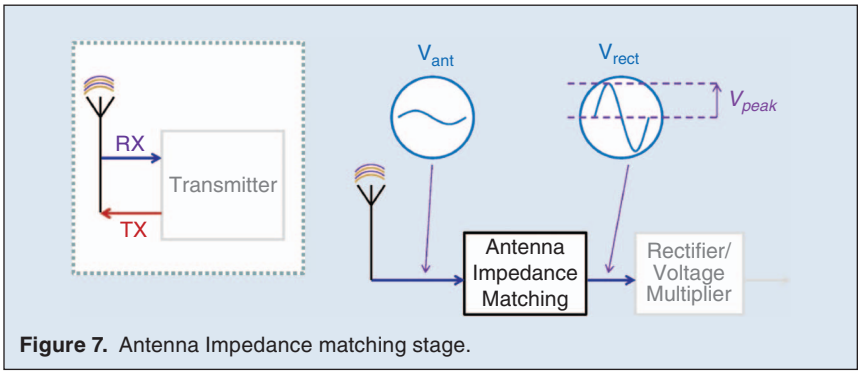


Figure 7. Antenna Impedance matching stage.

VII. Analysis: Antenna Impedance Matching

A common factor in any power harvester unit, whether the end application is RFID, ambient harvesting, wakeup or detection, is the use of an impedance matching network and a voltage multiplier. It is critical that these two circuit elements are approached through *co-design*, as the construction of each has a dramatic effect on the performance of their counterpart, and failure to properly model their relationship may result in substantial efficiency reduction through power reflection and stage threshold losses. To tune the circuit to application specifications, many publications examine the two elements independently before using an iterative optimization algorithm in simulation, revising circuit values until the best values are obtained [49]. Following this design pattern, this paper will approach the research on impedance matching and rectifier design as independent sections, which should be repeatedly examined throughout the design process to prevent inadvertent undermining of prior performance gains.

A. The Impedance Matching Network

Figure 7 shows the placement of the impedance matching stage. As the element directly responsible for antenna management and waveform tuning, the mathematics of the impedance matching network revolve around two figures of merit, the *reflection coefficient* and the *passive network voltage gain*. The reflection coefficient ensures that the circuit does not radiate power back into free space at the antenna aperture by precisely matching the real and imaginary impedances of the circuit, while the passive voltage gain provides a slightly higher V_{peak} at the rectifier to overshoot the threshold voltage V_{TH} and increase efficiency. These metrics are determined by the antenna *Characteristic Impedance*, the *Input Impedance* of the rectifier, and the *Quality Factor* of the matching network.

Impedance matching at the antenna refers to designing of a network of passive components that transform two mismatched impedances to equivalent ones. The matching of the antenna to the rectifier requires such a network to minimize the *reflection coefficient*, shown in (Eq. 13), which assists in modeling the amount of energy that will be reflected:

$$\text{Reflection Coefficient} = \Gamma = \frac{Z_{\text{rect}} - Z_{\text{ant}}^{*}}{Z_{\text{rect}} + Z_{\text{ant}}^{*}} \tag{13}$$

where $Z_{\text{ant}} = R_{\text{ant}} + X_{\text{ant}}$ is the antenna impedance, Z_{ant}^{*} is its complex conjugate, and $Z_{\text{rect}} = R_{\text{rect}} + X_{\text{rect}}$ is the input impedance of the rectifier stage. Thus, it can be seen that maximum power transfer (minimum power reflection) will occur when the resistive elements (R_{ant} and R_{rect}) are equal, and the reactive components (X_{ant} and X_{rect}) are of opposite sign [50]. Failure to achieve this case will result in some fraction of the total power being reflected away from the rectifier, quantified as the *Power Reflection Coefficient* $|\Gamma|^2$

$$\text{Power Reflection Coeff.} = |\Gamma|^2 = \left| \frac{Z_{\text{rect}} - Z_{\text{ant}}^{*}}{Z_{\text{rect}} + Z_{\text{ant}}^{*}} \right|^2 \tag{14}$$

Reflection of incident power at the antenna (i.e., $|\Gamma|^2 < 1$) reduces the available power to the rectifier, thereby decreasing the overall efficiency as shown below

$$P_{\text{avail}} = P_{\text{incident}} - P_{\text{reflected}} \tag{15}$$

As shown in Fig. 8, even well designed antennas that are designed to appear as the pure resistive industry standards $R_{\text{ant}} = 50\Omega$ or 75Ω may contain traces of inductive L_{ant} or capacitive C_{ant} parasitic impedance.

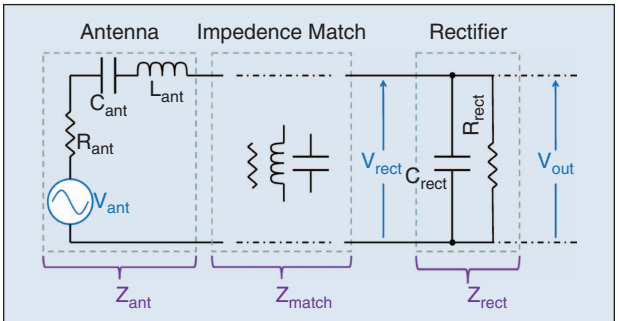


Figure 8. Impedance matching network.

Circuits seeking to maximize antenna absorption and voltage gain must carefully consider the tradeoffs created by the components in their matching network and the resonant traits of their arrangement.

The input impedance of the rectifier (Z_{rect}) includes a relatively large resistor (R_{rect}) at low power levels, and a small capacitive load (C_{rect}) due to the parasitic capacitances of the rectifying elements. The impedance matching network has an impedance of its own (Z_{match}), and is required to cancel the reactive units and deliver the power from the antenna resistance R_{ant} (also referred to as *radiation resistance*) to the load resistance R_{rect}. Several different methods of impedance matching are described in this section, which all attempt to implement Z_{match} using various topologies of LC components.

B. Passive LC Voltage Boosting

The primary responsibility of the LC matching network is to transfer the maximum amount of power from the antenna radiation resistance (R_{ant}) to the resistive portion of the rectifier (R_{rect}). LC matching network design must take into account the rectifier parasitic capacitance (C_{rect}) resulting from the input capacitance of the active devices used in the rectifier, such as Schottky diodes and MOS transistors. An observation of Fig. 8 reveals that, as long as $R_{\text{rect}} > R_{\text{ant}}$, a voltage boost at R_{rect} can be achieved in relationship to V_{ant}. The antenna incident power is $(V_{\text{ant}}^2/R_{\text{ant}})$. Once the matching network cancels out the reactive portion of the impedance between R_{ant} and R_{rect}, this power is shared between the R_{rect} and R_{ant}. Maximum attainable LC voltage boost (named "passive" voltage boost) is therefore [51]

$$\text{Passive Voltage Boost} = A_{\text{LC}} = \frac{V_{\text{rect}}}{V_{\text{ant}}} \leq \frac{1}{2}\sqrt{\frac{R_{\text{rect}}}{R_{\text{ant}}}} \quad (16)$$

C. Quality Factor (Q Factor) Analysis

Due to the threshold voltage drops and the power loss due to those drops, the effective input resistance of the rectifier is typically much lower than the calculated value under "ideal" assumptions, typically more than an order-of-magnitude or worse. Furthermore, the LC boosting circuitry consists of inductors that are constructed from metal wires inside an IC which contain resistive and capacitive parasitics. While the losses due to the capacitive portion of the parasitics can be eliminated by creating their complex conjugates during the impedance matching process, resistive parasitics simply create unpreventable power losses. This necessitates the definition of a *Quality Factor* metric, Q, that quantifies the potential for a component to efficiently store and deliver energy. For example, an inductor with inductance of L (i.e., a reactance of $X = \omega L$) and a series resistive parasitic R will have a Q as follows

$$\text{Inductor Quality Factor} = Q_L = \frac{X}{R} = \frac{\omega L}{R} \quad (17)$$

where ω is the frequency at which the inductor is working, in radians per second. Following the definition in Eq. 17, an ideal inductor with no resistive parasitics will store and deliver energy at 100% efficiency, i.e., $Q_L = \infty$. This is practically not possible, as every wire that the inductor is made out of will have some resistance. In an IC design, $6 < Q_L < 40$ are typical [14], [52], and $Q_L = 40$ is very good.

Q can be generalized to RLC networks as follows

$$\text{Quality Factor} = Q = 2\pi f \times \frac{\text{Energy Capacity}}{\text{Power Loss}} \quad (18)$$

where f is the operation frequency of the RLC network, *Energy Capacity* is the total amount of energy the network can store, and *Power Loss* is the continuous power loss endured by the resistive elements in the network. High Q values for the antenna impedance matching circuit improve the performance by boosting the voltage at the input at the rectifier, raising the V_{peak} and thus simultaneously improving the efficiency, sensitivity, and output voltage of the entire system. Circuits with a higher Q will oscillate with a greater amplitude, leading to a larger voltage gain at the output. Several studies have used this property to compensate for smaller antennas with a low radiation resistance, which causes a lower innate voltage amplitude at the antenna terminals. However, this improvement comes with some costs, specifically the non-trivial difficulty of evaluating Q values in complex matching networks, and the high component quality required to meet the stringent values required in these equations.

Q can be determined from the resistive and reactive elements of the matching network, but the exact formula will vary between configurations, and thus a matching circuit will have a Q value that is highly dependent on its topology. These equations can be extremely complex, and difficult to produce, even in simulation. Thus, a tradeoff between managable complexity and V_{peak} can occur in the design of this component. Q is also limited by the individual quality factors of the passive network components, which will have their own Q values, damping their

oscillation. Note that the low-power embedded technology used in RFID often severely limits component Q values, especially for inductors, leading many papers to disregard Q related bandwidth reduction as a negligible concern as no process can reach Q value where it would become relevant to the 902–928 MHz range. It is possible that this conclusion may change as circuit manufacturing for RF harvesting becomes more advanced, and extremely high Q components such as quartz L resonators become available for use in design [53], [54]. However, these limitations still present significant obstacles for designers hoping to leverage the Q boosting opportunities of LC circuits. By carefully designing the matching circuit, a voltage boost at the IC input can be achieved due to the high resistance of the load. The authors in [52] report a simulated voltage boost of 3 to 8 based on different parasitic values.

D. Impedance Matching Network Topologies

Figure 9 depicts most commonly used impedance matching networks, although many other configurations are possible by replacing certain capacitors with inductors, and vice versa. Additionally, more stages than what is shown in Fig. 9 can be utilized if a large bandwidth needs to be achieved by the LC network. All of these circuits, and many other alternatives of them exist to simply implement the Z_{match} described in Fig. 8. Although implementing Z_{match} is a straightforward task by using a Smith Chart as will be explained shortly in this section, different topologies have a dramatically different effect in the way parasitics are handled by the LC network. These topologies will be explained individually:

L Networks: The L network is named due to the way L and C components are connected in an L shape. This setup thus matches the antenna to the rectifier, and may also cancel out stray reactive impedance. At the selected circuit frequency, this equivalent circuit will appear as a resonant LC tank, with a resistive load matched 1:1 with the input resistance to maximize power transfer.

π and T Networks: Many alternatives to the L network exist, which utilize different arrangements of passive components to perform the same mathematical transformation of apparent impedance. These alternatives are *π networks*, *T networks*, or even more complex arrangements with many stages of capacitors and inductors. These networks do not alter the final impedance match, but instead alter the *Quality Factor* of the network, thereby potentially improving the passive voltage boost, A_{LC}.

Inductor-Only Networks: In response to tradeoffs and limitations in designing L networks, studies such as Barnett et al. [47] have questioned the use of LC passive voltage boosting. Under certain conditions where the apparent load resistance has been reduced and the radiation resistance of the antenna is high, the ratios used in the evaluation of Q will be low, and the matching network will not provide much additional passive voltage boosting regardless of the network topology. Additionally, when integrated into standard CMOS processes, many microscale passive components have a low Q, defined as their intrinsic reactance over resistance. Thus, the advantages of passive voltage boosting may be lost, or worse, the Q factor will actually attenuate voltage gain. Barnett et al. [47] have suggested that a standard L network be replaced by a simple *Shunt* or *Series* inductor or a 1:K transformer, as shown at the bottom of Fig. 9. These designs will provide no voltage boosting, but can be cheaper to manufacture and test, and will be more efficient when paired with high-power loads that appear as a small resistance at the entrance of the rectifier.

Transformer-based Networks: A study by Soltani et al. [51] has investigated the use of a CMOS-process integrated 1:N transformer and a capacitor as an impedance matching network, shown on the bottom right of Fig. 9. Transformers make use of a pair of coupled inductors that perform voltage magnification and resistive transformation relative to their coil ratio via induction. Note the difference between Soltani et al. [51] who uses an additional capacitor, effectively making it an LC network vs. Barnett et al. [47] who only use a transformer. Thus, Soltani et al. can provide both voltage step up and resistive matching simultaneously, augmented by reactive components at each end to form dual LC tanks and cancel unwanted reactances. While transformers have long been used for impedance matching in radio applications, they are not usually seen as practical at the frequencies required for RFID due to implementation

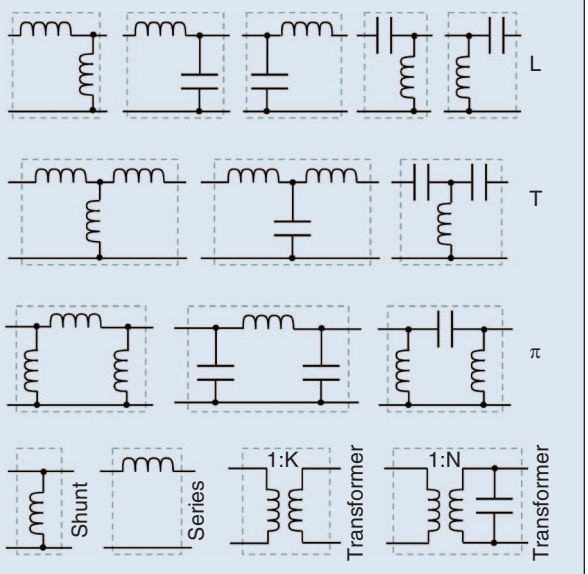


Figure 9. Different impedance matching network topologies: L networks, T networks, π networks, single inductor and Transformer-based networks.

cost and core losses. However, when integrated on chip or in limited-issue applications where cost is not an issue, transformer use may lead to efficiency gains and holds potential for future research.

As matching network performance is dependent upon a number of factors, including component quality, chip process, cost, size, and frequency, no superior option can be recommended for any given application. Circuits seeking to maximize antenna absorption and voltage gain must carefully consider the tradeoffs created by the components in their matching network and the resonant traits of their arrangement. Once a design philosophy appropriate for a specific application has been decided upon, a complementary rectifier can be chosen and co-optimization of these two units can begin. This rectifier element has the most research history of any section of the wireless power harvester, and is discussed at length in Section VIII.

E. Smith Chart-Based Matching Network Design

A Smith Chart is possibly one of the most practical and intuitive design tools to implement impedance matching networks and can be applied to any one of the topologies shown in Fig. 9. An example Impedance Smith Chart is shown in Fig. 10, which contains four different types of circles that traverse a constant resistance (r), constant reactance (x), constant conductance (g), or constant susceptance (b). Every point on the Smith Chart denotes an impedance value $z = r + jx$, and a corresponding admittance value $y = g + jb$. Note our lower case notation, which implies normalized impedance and admittance values, by computing $z = Z/Z_{\text{ant}}$, or more generally the characteristic impedance of the source (e.g., $50\,\Omega$). This normalization allows us to use the Smith Chart independent of the frequency.

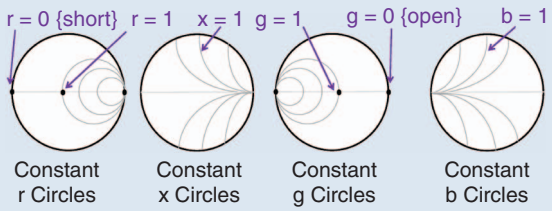


Figure 10. An impedance Smith Chart with four different types of circles to convert between normalized impedance ($z = r + jx$) and normalized admittance ($y = g + jb$) throughout the impedance matching process.

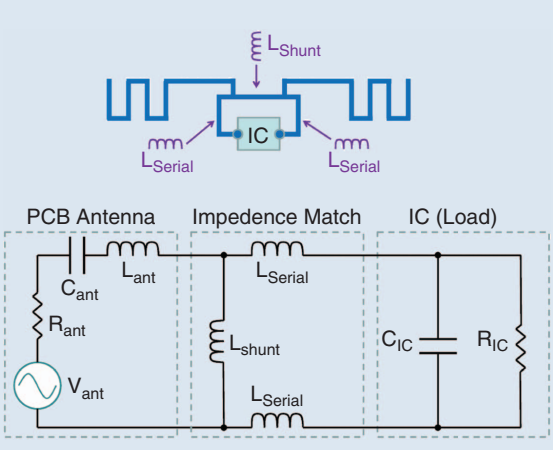


Figure 11. A PCB-printed meandered dipole antenna and an impedance matching circuitry built using three impedances that are a part of the PCB pattern [28].

Inductors add to the reactance and do not change the resistance (ignoring the parasitic resistance). Therefore, adding a series inductor to a circuit is equivalent to moving the current impedance "up" a constant resistance circle, during which, we move from $z = r + jx_1$ to $z = r + jx_2$. The contribution of the inductor to the x value is $x_2 - x_1$, thereby allowing us to calculate its inductance. Series-connected capacitors perform an identical transformation, except, they add negative reactance, thereby traversing a constant-resistance circle in the "down" direction. Shunt-connected inductors and capacitors are identical, except, they add to the admittance, rather than impedance. Therefore, to compute the contribution of a shunt-connected element, it would make the most sense to switch to the admittance and use the constant g curves. Using these curves, inductors still move us up, and capacitors move us down. The goal of the design of an impedance matching network is to determine a list of shunt/series capacitor/inductor elements to start at the source impedance and end up at the load impedance.

Algorithm 1 Methodology in using an impedance/admittance Smith Chart (shown in Fig. 10) to design an impedance matching network.

1. Normalize the source impedance Z_{ant} to get z_{ant}
2. Normalize the load impedance Z^*_{load} to get z^*_{load}
3. Plot z_{ant}, z^*_{load} on the Smith Chart
4. The goal is to go from z_{ant} to z^*_{load}
5. During traversals, use one of the four types of circles
6. Series elements: use constant r, constant x circles
7. Shunt elements: use constant g, constant b circles
8. Inductors move us up. Capacitors move us down.
9. At any point, to convert from z to $y = 1/z$, use the corresponding $\{r, x\}$ vs. $\{g, b\}$ intersection
10. Keep traversing circles until you reach z_{load}.
11. The elments you used is the matching network

Algorithm 1 shows the impedance matching methodology using a Smith Chart. An example will clarify this methodology: Dobkin [28] shows a PCB-printed meandered dipole antenna construction with a total antenna width of 9 cm using the configuration in Fig. 11.

Radiation resistance of the antenna is $R_{\text{ant}} = 25\ \Omega$. Operating frequency is 860–960 MHz. Antenna parasitics are $C_{\text{ant}} = 0.45$ pF, $L_{\text{ant}} = 63.5$ nH, which cancel each other out at 940 MHz. Therefore, we will assume a pure resistive antenna resistance of $Z_{\text{ant}} = 25\ \Omega$. The IC load (i.e., input of the rectifier) is $R_{\text{IC}} = 2200\ \Omega$, $C_{\text{IC}} = 1.1$ pF. This requires PCB-printed matching inductors $L_{\text{serial}} = 11$ nH and $L_{\text{shunt}} = 4$ nH.

Let us calculate this matching circuitry for Fig. 11 using the methodology in Algorithm 1. The antenna impedance is $Z_{\text{ant}} = 25\ \Omega$, and the normalized antenna impedance is $z_{\text{ant}} = 1.0$, which is the dot right in the middle of the Smith Chart in Fig. 12. $Z = 2200\ \Omega \parallel 1.1$ pF is the load. Computing the normalized load impedance, we get $z_{\text{load}} = 0.45 - \text{j}6.15$. So, $z^*_{\text{load}} = 0.45 + \text{j}6.15$. This is what we are trying to end up with, since, if we end up with $z^*_{\text{load}} = 0.45 + \text{j}6.15$, the $\pm\text{j}6.15$ will cancel each other out, and the antenna will appear pure resistive $(z = 0.45)$ to the load, thereby allowing maximum power transfer. This is a fairly simple transformation and only two elements are needed: one shunt inductor L_{shunt} and one series inductor L_{series}, as shown in Fig. 11. The reason for two series inductors appearing in this figure is since the final value of the inductor is implemented as two symmetric wires (each with half the value) as shown in the meandered antenna drawing.

Let us now design the network using a Smith Chart step by step. First, since there is a shunt inductor, it is a lot easier to deal with admittance and conductance. Our starting point is $y = 1$ for the antenna. Therefore, $g = 1$ and $b = 0$. A shunt inductor will not change g, but, will add a negative value to b. So, we traverse the $g = 1$ constant conductance circle until we intersect a point that can help us with our next move. Anticipating that, our next move is to add a series inductor, we are trying to get to a point which has the desired $r = 0.45$ value. This is since we have only one more move left, and we want to end up with a $z^*_{\text{load}} = 0.45 + \text{j}6.15$. The effect of adding the shunt inductor is moving along the constant $g = 1$ and ending up at $y = 1 - j1.1$ as shown in the left-directed arrow. From this move, we know that, the shunt inductor added -j1.1 to the susceptance, and the corresponding value can be calculated from $2\pi fL = 1/1.1 \times 25$. Note that, the L we calculate here is the actual value, since multiplying by 25 reversed the normalization. We get $L_{\text{shunt}} \approx 4$ nH.

Step 2 is to determine the series inductor. For this, it is easier to use impedance and resistances. To convert the current impedance we have, we can either calculate $(1 - j1.1)^{-1}$ or simply look at the intersecting impedance point, which is 0.45+j0.5. From this point, we are trying to go to $z = 0.45$+j6.15. This traversal is depicted by the second right-directed arrow which keeps $r = 0.45$ constant and adds j5.65 to impedance. The value of an inductor that can realize this can be calculated from: $2\pi fL = 5.65 \times 25$, which is $L \approx 22$ nH. When we implement this inductance with two symmetric wires, each end up being is $L_{\text{series}} = 11$ nH.

F. Antenna Design

Since RFID antennas are built directly into the RFID tag, their design plays a crucial role in the overall RFID tag performance. Small parasitic capacitance and inductances cannot be prevented when designing a PCB-printed antenna. Rather than trying to eliminate them, it is common to regard them as a part of the LC impedance matching circuitry [43]. While elaborate antenna design techniques are outside the scope of this paper, a rich base on information is available [36], [37], [40], [55]–[58]. In this paper, we aim to cover the basics of antenna types and their effect on the LC impedance matching.

Monopole/Dipole Antennas: Figure 13 depicts common PCB-printed antennas that are incorporated into an RFID tag as part of the PCB design [42]. Monopole antennas have a single feed point, whereas dipole antennas have two symmetric feed points. Typical effective end-to-end distances for monopole antennas are $\lambda/4$, whereas dipole antennas consist of two $\lambda/4$ wires, totalling $\lambda/2$ end-to-end. The top two dipole designs take advantage of the circles printed on the PCB to extend the effective length of the antenna. For example, the top one has an effective dipole length of 9.5 cm, corresponding to $\approx \lambda/4$ at 915 MHz (see Table 2). While $\approx \lambda/2$ is the ideal length for dipole antennas, smaller sizes will work, albeit at the expense of reduced harvested power [45].

Balanced/Unbalanced/Balun: An important observation from Fig. 13 is that, since monopole antennas have only a single feed point, they are referenced to a Ground

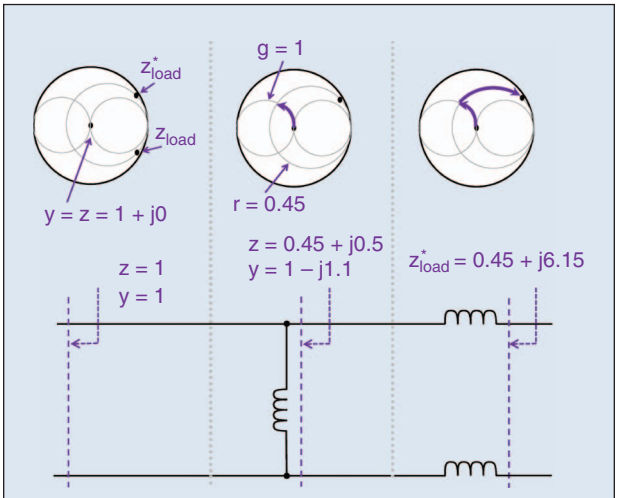


Figure 12. An example Smith Chart implementation. The constant r and constant g circles show the effect of adding shunt and series inductors.

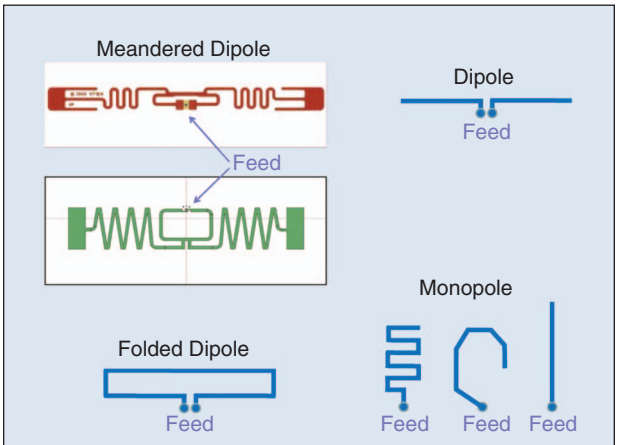


Figure 13. PCB-printed monopole and dipole type antennas.

(GND), which is shared by the rest of the digital circuitry. Alternatively, dipole antennas provide two symmetric feed points, thereby generating a signal that doesn't need an additional reference point such as GND. For this reason, the GND-referenced single-ended signals are called *Unbalanced*, whereas symmetric (differential) signals generated by dipole antennas are called *Balanced*. Since the digital circuitry inside the RFID IC will need a GND reference, a conversion from balanced-to-unbalanced is needed when the antenna provides a balanced feed. This conversion task is achieved by simple passive LC-based circuitry that is called a *Balun Converter*. A simple Balun circuit is shown in Fig. 14, which converts a 50 Ω unbalanced antenna input to a balanced differential voltage, which is fed into an IC that needs balanced inputs [59].

Electrically Small Antennas (ESAs): Breed [44] provides example ESA (Electrically small antenna) designs, which are shown in Fig. 15. The most common definition

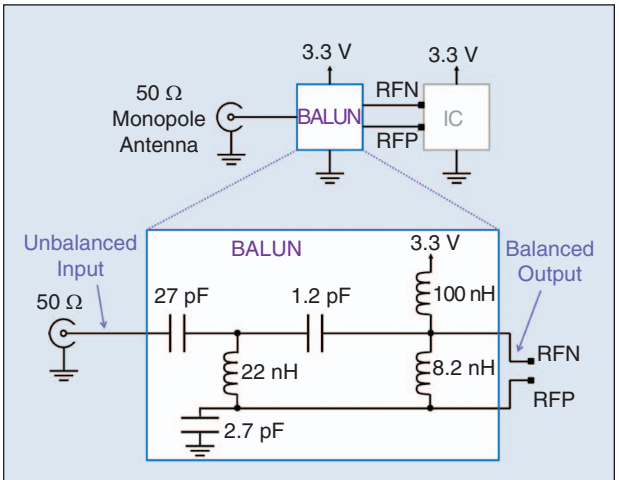


Figure 14. A 915 MHz Balun converter (below) converts a GND-referenced 50 Ω antenna voltage (unbalanced) to a balanced voltage which is applied to an IC (above).

of an ESA is an antenna whose dimensions do not exceed $\lambda/10$, in terms of length, diameter, or diagonal length for patch antennas. Therefore, ESAs are utilized heavily in designs where space is premium, such as RFID tags. In Fig. 15, an ESA Dipole and loop antenna design are shown with no dimension exceeding $\lambda/10$. The computed impedance of the dipole ESA is $Z_{\text{ant}} = 1.96\,\Omega - j1758$, thereby making this a capacitive antenna with radiation resistance $R_{\text{ant}} = 1.96\Omega$ and the capacitive portion $C_{\text{ant}} = 0.9$ pF @100 MHz. Alternatively, the loop ESA has a $Z_{\text{ant}} = 3.0\,\Omega + j800$, which implies an inductive antenna.

Although ESAs are small, their gains are comparable to that of $1/2\lambda$ antennas. However, due to the small size of the ESAs, their radiation resistance is very low and the capacitive (or inductive) portion of their impedance necessitates the usage of large size inductors and capacitors in the LC matching network to create the complex conjugate of their impedance. To exemplify this, refer to Fig. 15, where an impedance matching network for a dipole ESA requires capacitance values that are 50 times the antenna capacitance in the matching network. Inductors are also very large. To exacerbate this disadvantage, these large inductor and capacitances in the matching network have parasitic resistances which cause power dissipation, thereby reducing the efficiency of the ESA.

G. Design Examples: Antenna LC Matching

Figure 13 shows different types of antennas with different shapes printed on the PCB. A commonly used PCB-printed type antenna is a *meandered dipole antenna* which provides a balanced output and is constructed using zig-zagged patterns to save valuable PCB space. An example of such an antenna is shown in Fig. 11, which has an effective length of $\lambda/2 \approx 15$ cm, although it only has a width of ≈ 9 cm on the PCB. Such a construction will have a parasitic capacitance C_{ant} and a parasitic inductance L_{ant} in addition to its radiation resistance R_{ant}. The complex part of the impedance created by these parasitics can be eliminated by building a three-inductor structure using two serial inductors and one shunt inductor on the PCB, named L_{serial} and L_{shunt}, respectively in Fig. 11. The complex part of the impedance of this three-inductor structure is the conjugate of the antenna impedance, thereby resulting in a net pure resistive, applied to the load. Note the parasitic capacitance C_{IC} at the input of the IC due to the input capacitances of the rectifier circuit.

Example: Papotto et al. [60] describe a 90 nm CMOS IC design with a built-in matching network inside the IC. This IC is powered from an external 50 Ω antenna, and the matching network provides its output to the rectifier section, which has an input load impedance of (760 Ω ‖1.5 pF). Inside the IC, the parasitic bonding capacitance is calculated to be $C_{\text{bonding}} = 300$ fF and the

bonding inductance is calculated to be $L_{bonding} = 2$ nH, with Q ≈ 20 @900 MHz. The matching network has a shunt inductor $L_{shunt} = 6.8$ nH and a total series inductor $L_{series} = 11$ nH, both with a Q = 12.

Example: Assume that $P_{incident} = -16$ dBm, which equates to 25 μW. On a standard 50 Ω antenna, this would result in a $V_{ant} = 35.4$ mV RMS antenna voltage, i.e., a sine wave oscillating between peak amplitudes ±50 mV. Recall from Section VI-C that, this translates to $V_{peak} = 50$ mV. Let us further assume that, the digital portion of the circuit is working at $V_{DD} = 1.4\,V$ and the regulator dropout voltage is $V_{dropout} = 100$ mV. Therefore, from Eq. 7, we have $V_{out} = 1.5\,V$, which implies that, we need to deliver a sinusoid antenna voltage with a ±50 mV peak to the rectifier output @ DC 1.5 V. If we assume that, the rectifier stages provide a 6x voltage boost (from 250 mV peak to 1.5 V), the rest of the boost, 50 mV peak to 250 mV peak ($A_{LC} = 5$), must be realized by the passive LC matching network.

To calculate what the rectifier input load (R_{rect}) would be seen as, in the example above, let us assume a System PCE of $\eta_o = 10\%$, which means that only 2.5 μW of the incident 25 μW is being delivered to the IC at $V_{DD} = 1.4\,V$ and $I_{DD} = 1.785\,\mu$A. Next, we need to calculate the input current of the rectifier to be able to calculate its power draw from the LC network output. From Eq. 12 we know that, 10% is the product of three distinct efficiencies: From Eq. 11, Regulator efficiency is 1.4/1.5, which is $\eta_{reg} = 0.93$. From Eq. 9, the antenna will use at least as much power as what is delivered to the rectifier input, plus more LC network losses will be incurred due to the resistive parasitics, so, $\eta_{ant} = 0.4$ is a reasonable assumption. Therefore, the efficiency of the rectifier from Eq. 12 is $\eta_{rect} = 0.269$.

According to Eq. 10, we calculate $P_{rect} = 9.95\,\mu$W RMS. This computes $R_{rect} = 0.25^2/(9.95 \times 10^{-6}) \approx 6.28\Omega$. However, the effective R_{rect} will be much smaller than this due to the fact that the RMS value of the rectifier input current will exhibit a power consumption pattern that consists of large dead time intervals followed by more intense peaks when the $V_{rect} > V_{TH}$. This example shows that, the incident 25 μW power was delivered to the load after a 22.5 μW loss within the circuit. 15 μW is consumed (25 μW × 0.6) to provide backscattering communication and due to the resistive losses within the LC matching network, delivering ≈10 μW into the rectifier. The rectifier wastes 7.31 μW of this power, delivering only 2.69 μW into the regulator. The regulator burns 0.19 μW and delivers 2.5 μW to the load.

VIII. Analysis: Rectifier/Voltage Multiplier

Of all the components of the wireless power harvester, the rectifier element has by far the most research history and design emphasis. The placement of the rectification and voltage multiplier stage is shown in Fig. 16. Many changes have occurred to the design of RF rectifiers over the years, often driven by changes to process technology, legal regulations, and new standards for RF transmission. In this section, a detailed analysis of the development of these rectifiers is assembled from the body of historical research, starting from the simplest rectifier elements to the multi-stage, digitally managed versions that are examined today.

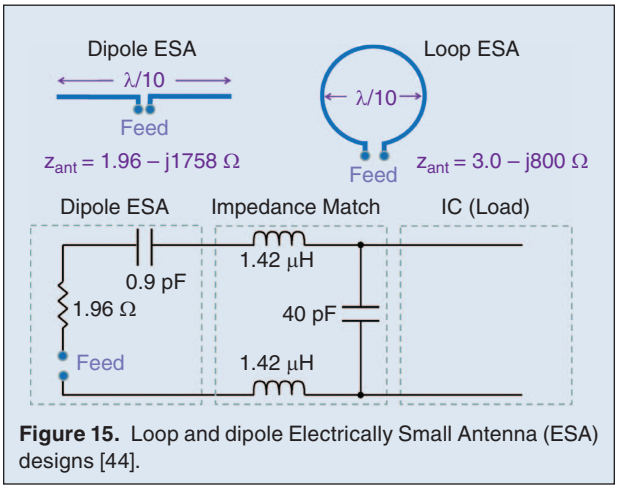


Figure 15. Loop and dipole Electrically Small Antenna (ESA) designs [44].

A. Basic Rectifiers

Once a signal has been transformed by the impedance matching network, the rectifier/multiplier of a wireless power harvester serves to both rectify the signal to DC power and boost the voltage from the antenna (often in the low mV range) to a useful level for digital operation. At far field ranges of 5 m, this invariably necessitates stacking several rectifiers into a multi-stage multiplier, expanding the typical rectifying *RF envelope detector* into a system more analogous to the *charge pumps* used in VLSI design.

When examined in the literature, the structure of the multiplier is often regarded as the most critical component of the RF power harvester, as it represents the largest source of unavoidable power loss and thus its design dictates the sensitivity, efficiency, and overall instrumental quality of

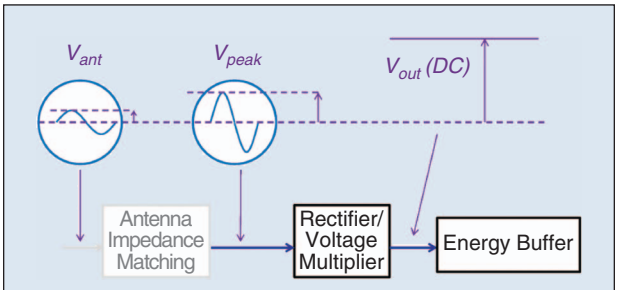


Figure 16. Voltage Multiplier/Rectifier stage.

the circuit. However, it is also the most difficult element to model, since the nonlinear behavior of most charge pumps at high frequencies can have unforeseen capacitive and resistive effects, causing unpredictable changes to the behavior of the LC matching network and the back-end energy storage. In addition, the threshold V_{TH} of the rectifiers' diode components will massively affect the performance of the circuit, as its relationship to the V_{peak} at the initial terminals of the rectifier will determine both the sensitivity and efficiency of the entire multiplier. When used in high power operations, V_{TH} is often so minuscule that it is disregarded (e.g., 150–200 mV), but under the extreme low power conditions of RFID, V_{TH} is often on a comparable level to the input voltage at the terminals of the first stage, and thus providing insufficient terminal voltage will result in the entire system being starved of power. Advanced structural designs should attempt to both reduce V_{TH} and improve the total multiplier gain through intelligent capacitor placement, an optimized number of stages, and carefully calculated biasing. To further these goals, a number of different rectifier structures and technologies have been explored and implemented over the years, each of which will be addressed in order of complexity.

The simplest implementation of an RF rectifier is shown in Fig. 17a. As the sinusoidal input of the antenna enters the positive peak region, the diode will conduct and produce a positive voltage across the capacitor, charging the capacitor and providing charge to the output simultaneously. When the sinusoidal enters the negative valley region, the diode will cease to conduct and the capacitor will supply all of the charge to the output. The net effect of this operation is a DC voltage on the capacitor terminals with some ripple, thereby corresponding to *rectification*.

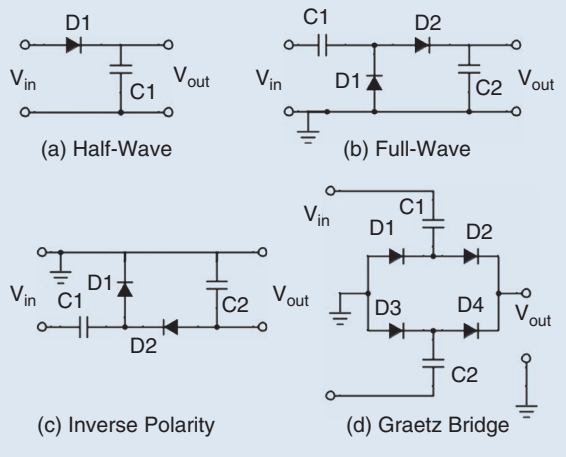


Figure 17. Basic rectifier constructs: a) Half-wave detector, b) full-wave rectifier, c) inverse-polarity rectifier, and d) Graetz bridge.

This extremely simple model only performs half wave rectification, and is more typically replaced with the circuit of Fig. 17b, which rectifies both the negative and positive regions of the RF signal to provide a more efficient and stable DC output. This rectifier may also be used in the opposite polarity, as shown in Fig. 17c. These three types of rectifiers turn a sine wave oscillating between $\pm V_{peak}$ volts to a DC voltage that is V_{peak}. The bridge rectifier shown in Fig. 17d forgoes the use of internal capacitors to output the full peak to peak voltage of the signal, providing double the voltage of the prior rectifiers, $2 \times V_{peak}$. However, this rectifier cannot be referenced to a common ground (GND) at both the input and output.

These simple rectifiers do not provide any form of voltage gain, and can only generate an output DC value proportional to the amplitude of the incoming RF signal. Circuits that only utilize a single stage rectifier are typically referred to as *rectennas*, a term coined by William C. Brown in 1964 for the integrated use of an antenna and rectifying diode assembly. Due to their lack of stage losses and predictable behavior, rectennas can be tuned to great efficiency in RFID assembly, and are especially useful in communications detection where contrast is more critical than amplitude [61]–[63]. However, the voltages produced by rectennas are typically not sufficient to power an IC at far field ranges, as most rectennas cannot achieve a voltage over 1V at input power of 0 dBm or lower. Thus, power harvesters used for powering CMOS digital circuitry must cascade rectifier stages to achieve the voltages necessary for digital transistor function.

B. Multistage Rectifiers

The displayed diagrams of the Dickson (Fig. 18a) and Villard (Fig. 18b) voltage cascades (also known as the Greinacher and Cockcroft-Walton multipliers, respectively) are both the simplest and most commonly used of the multistage designs. While both designs are based on the established full wave rectifier, the difference lies only in how the capacitors are connected. Dickson ties each stage capacitor to GND, whereas the Villard references each stage to the prior unit. Voltage clamping via the capacitors establishes a new reference voltage for each stage, allowing the subsequent stages to further multiply the total voltage value. A study done by [64] contends that there is no significant performance difference between the Dickson and Villard approaches. However, when examined at small signal, the Dickson presents a significantly easier nonlinear impedance analysis, and is thus used more commonly than the Villard high frequency designs where codesign with the antenna is essential. As an alternative to series connection, these rectifiers may also be assembled in parallel using stacked rectifiers of opposing polarity (Fig. 18c). Several studies

[46], [51], [65] have shown that this method has beneficial effects on efficiency by reducing the number of stages and simplifying parasitic effects. However, note that this mirrored configuration has a floating output in the same manner as the bridge rectifier, and cannot be referenced to a common GND at both the input and output ports.

Matching for multistage circuits can be a significant challenge, but models for predicting their impedance and output voltage have been compiled by many studies for use in both theory and simulation. Early studies, including the very first exploration of the topic by Dickson et al. [66], utilized a simple linear analysis of the design with marginal accounting for the capacitive parasitics at each stage (Eq. 19). This equation was mirrored in many of the first papers discussing the use of power harvesting for RFID [14], [67], though it was quickly noted that the frequency dependent components of the equation would become negligible at UHF frequency, leading to the simplified Eq. 20. Adapted versions were later developed for the dual polarity Greinacher designs, which have double the gain per stage [46].

$$V_{DC} = V_{IC}\left(\frac{C_C}{C_C - C_S}\right)N - \frac{I_{LOAD}\cdot N}{(C_C + C_S)\cdot f} \tag{19}$$

$$V_{DC} = N\cdot(V_{p,RF} - V_d) \tag{20}$$

where V_{DC} is the output voltage of the cascaded multiplier, $V_{p,RF}$ is the peak voltage of the RF signal, and V_d is the voltage drop on the diodes.

However, later studies noted certain flaws in these models, stemming from inconsistent consideration of the different operating states of the nonlinear components and the effect of parasitics on each stage. Studies by [68] and [69] examined the Dickson multiplier from a nonlinear perspective, utilizing a modified Bessel solution to create a more accurate model of the stage behavior. These models were further developed by [70], which included non-ideal traits into the model structure, and [47], which adapted the model to include LC matching effects. Unfortunately, these later models are extremely complex and in many cases are only solvable using numerical iteration and advanced computation algorithms. For this reason, modern rectifier design is now done almost entirely through simulated analysis, with the aid of iterative testing algorithms [49].

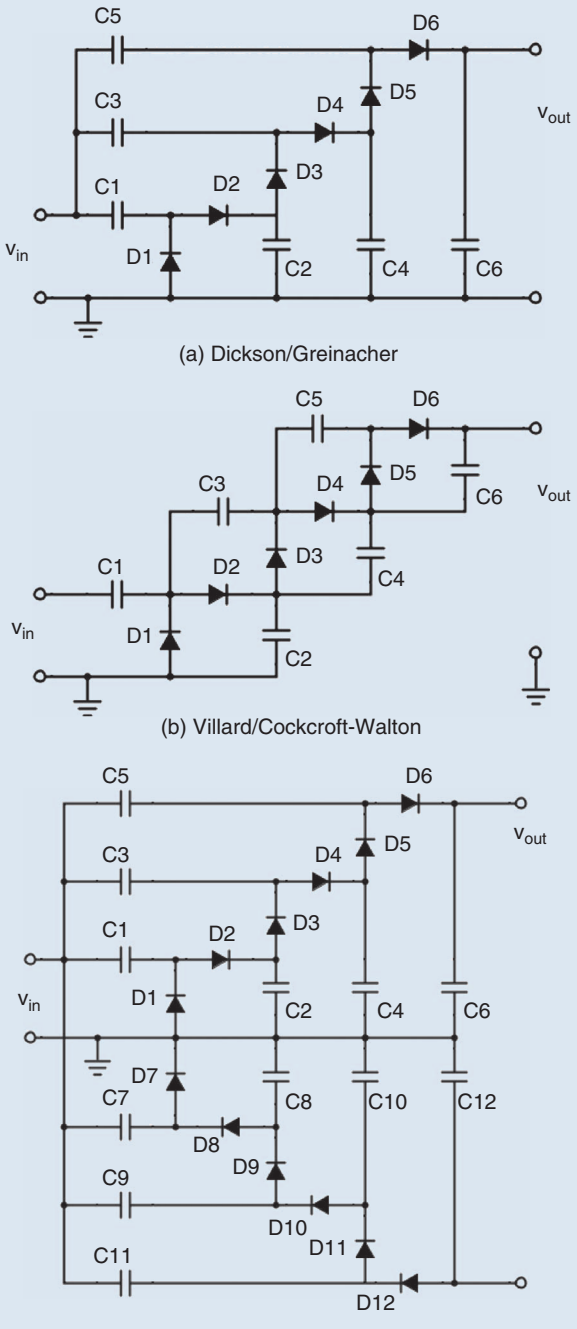
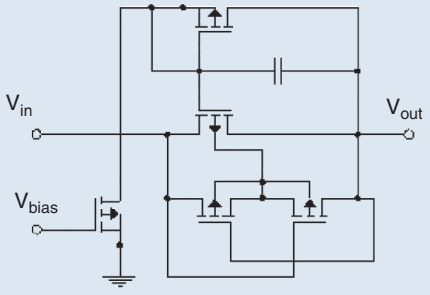


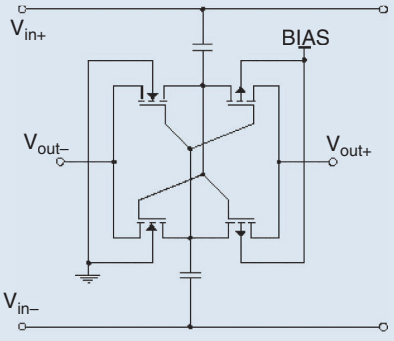
Figure 18. Different types of cascades: a) Dickson/Greinacher cascade, b) Villard/Cockcroft-Walton cascade, and c) Mirrored Greinacher cascade.

C. Schottky Diodes vs. Diode-Connected MOS Transistors

The rectifiers above are shown using diode components for ease of interpretation. Schottky diodes formed the basis of early rectifier designs [14] for their low threshold voltage, exponential voltage drop with current, and stable performance under varying temperatures. The Schottky diode remains in use for modern rectifiers, especially for those built with discrete components [71], [72], since they are often available as surface mount packages and can thus be used in a PCB design. Several studies have achieved improved results simply through updated Schottky process technology [67], [73], and performance can be expected to continually improve as the process technology advances over time.



(a) NMOS-Based Diode Emulation



(b) Differential Drive Stage

Figure 19. Process alterations : a) Diode emulation by using multiple transistors, b) differential drive stage.

However, many publications have opted not to use Schottky diodes due to their expense, inconsistent process quality, and difficulty to integrate into standard CMOS production. The diode connected transistor was introduced early on as an alternative [42], [74]–[76], but suffers a number of disadvantages when compared to the Schottky diode; transistors have a more significant initial threshold voltage that decreases quadratically, rather than exponentially like the Schottky, and experience more power loss over their nonlinear stages of operation [77] due to the body effect. Lowering this transistor threshold requires establishing a substrate bias appropriate for the transistor's position in the rectifier circuit. Early attempts to solve this problem [78] included more sophisticated diode emulation using multiple transistors to dynamically bias the substrate (Fig. 19a), or an *Internal Voltage Cancellation* (IVC) circuit overhead to dynamically assign the substrate value based on position; however, these efforts required substantially increased circuitry volume, and often needed an intensive pre-charging period before the biasing overhead could become active. More recent studies have partially offset these problems by using floating gate transistors with embedded charge [49], a process that substantially reduces V_{TH} and enhances efficiency, but requires high power pre-programming and may be vulnerable to performance losses over time as charge dissipates within the substrate material.

Several studies have foregone diode emulation altogether and have utilized transistor specific designs that *self-reference* their gate switching against later nodes in the rectifier. Early iterations of this concept, referred to as a differential drive multiplier, utilized the structure shown in Fig. 19b. The first-order differential drive multiplier significantly improved efficiency over prior CMOS designs [79], and could be further enhanced via engineered bulk biasing [80] and dynamic switching between series and parallel for improved impedance matching [81], [82]. The method of biasing gate terminals using later stage nodes was formally defined by [60] as *self-compensation* and can be implemented in more complex second and third order configurations that can further decrease threshold voltages.

D. Design Tradeoffs

It is difficult to categorize which rectifier design is ideal for any particular approach, given that each design has tradeoffs that may or may not be acceptable for a given application. However, several simulated comparisons have been done to categorize each structure, which may ease the selection process for uncertain designers [83]. In general, diode based rectifier designs have significant advantages due to the intrinsically superior threshold and parasitic traits of the Schottky junction, and will perform better when implemented in discrete designs or applications where size and cost are less of a concern. However, several techniques exist to improve the efficiency of CMOS rectifiers, and recent designs can achieve a significantly lower footprint and mass production cost for a comparative efficiency level.

It should additionally be noted that there is a direct relationship between the number of stages in a rectifier and the tradeoff between sensitivity and efficiency. Rectifiers with a higher number of stages provide higher voltage multiplication and lower the threshold voltage of their first unit, leading to increased sensitivity; however, they do so at the cost of higher power losses across the added stage components. Rectifiers with few stages have dramatically lower power losses, but may struggle to reach the required value of V_{out} at long ranges, and inevitably have a higher V_{TH} cutoff point where the rectifier ceases to function altogether. Extremes of both varieties can be seen in typical rectenna designs [48], [84], [85], which contain only one stage, and the sensitivity-focused power harvester of [43] which explores stage numbers of 10 or more. This tradeoff may necessitate application specific selection of the stage number to reach both acceptable range and power values.

E. Design Examples: Rectifier/Voltage Multiplier

Example: Shameli et al. describe a custom fabricated IC [52] using a TSMC 0.18 μm CMOS process, which is shown

in Fig. 20. The goal of the design is to match the impedance seen by the antenna to the resistive portion of the antenna R_{ant}, as shown on the bottom part of the figure to assure maximum power transfer. Impedance matching is done by designing an inductor inside the IC (top left of Fig. 20). This inductor has multiple parasitics. The equivalent circuit for the inductor is shown on the top right. This 23.3 nH inductor occupies a $455\,\mu$m $\times$ $455\,\mu$m die area and has a Q = 6.8 @920 MHz. Higher Q values mean, lower losses due to parasitics.

The power input of the RFID tag is $P_{in} = -14.1\ dBm$ ($38.9\,\mu$W). After matching and rectification, the power delivered to the IC is $P_{IC} = 2\mu$W, where $V_{DD} = 1V$ and $I_{DD} = 2\mu$A. This corresponds to a load of $R_{IC} = 500\ k\Omega$. The rectifier in [52] was constructed by using 8 diode-connected transistors (i.e., 4 charge pump stages). Increasing the number of stages to 5–8 does not improve the efficiency, in fact, it reduces it due to the added parasitics of the additional stages. Alternatively, decreasing the stages to 1–3 reduces the efficiency due to the lower voltage output of the harvester. Four stages (i.e., 8 NMOS diode-connected transistors) is therefore reported to be the optimum choice, yielding an overall PCE $\approx$5% for this design.

Example: Mansano et al. [86] provide simulations of an RF harvester using a 90 nm IBM 9RF technology. They also implement their IC using AMS 0.18 μm. They report their results on 13.56 MHz, 433 MHz and 915 MHz operating frequencies. At 915 MHz, they report N = 5 as the optimum number of rectifier stages, where each stage consists of a MOS transistor. For N $>$ 5, the efficiency goes down, which is consistent with most other reported results. At $R_L = 500\ k\Omega$ and $V_{DD} = 0.9\,V$, PCE $\approx$10% is reported @ $P_{RFin} = -20$ dBm. At N $<$ 5, the output voltage is lower, which in turn reduces the efficiency.

IX. Analysis: Power Management

The output of the rectifier represents the conclusion of energy *harvesting* and the beginning of energy *management*. The stages responsible for power management are outlined in Fig. 21. The circuitry placed at this terminal is responsible for maintaining a steady and continuous stream of power to the digital IC, preventing voltage spikes, power dropouts, excessive ripple, or any other unwanted characteristics that could disrupt digital performance. Some power management circuits may contain nothing but a voltage limiting zener diode; others may contain complex arrays of active and passive elements that store power, emulate resistance, and dynamically regulate voltage.

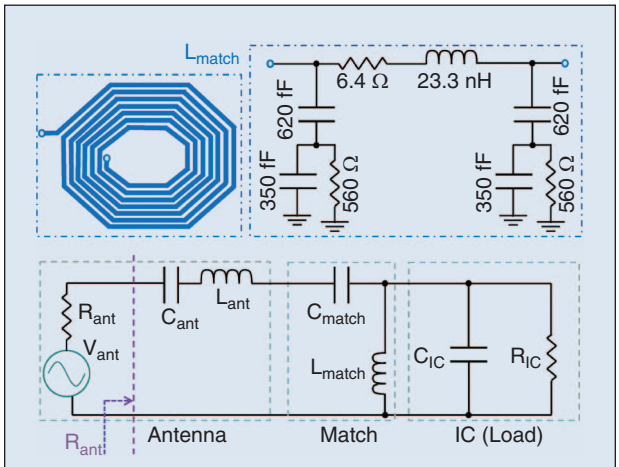


Figure 20. Impedance matching using a built-in inductor inside an IC [52].

The decision of what power circuitry to use is tied to the circuit application. The methods for a diversity of applications and their design-based tradeoffs are discussed over the course of this section.

A. Buffers and Limiters

Virtually every power harvesting circuit contains a *buffering* and *limiting element* at the output terminal of the rectifier. These elements are critical for maintaining performance over a wide range of input power, which will vary based upon range and transmitter strength as discussed in Section IV. At low power levels, the power at the rectifier output may be sporadic and will require a buffer to remain consistent, whereas high power outputs may induce electrical overstress in the IC if it is not protected by a limiter. While these end goals are fairly straightforward, the most efficient methods for implementing them have been the subject of considerable research.

Buffering elements are responsible for storing sufficient power to maintain the IC over brief periods of harvester inactivity, or to extend active operation by storing power over a longer period of pre-charging. Buffers can also serve to smooth the transient response of

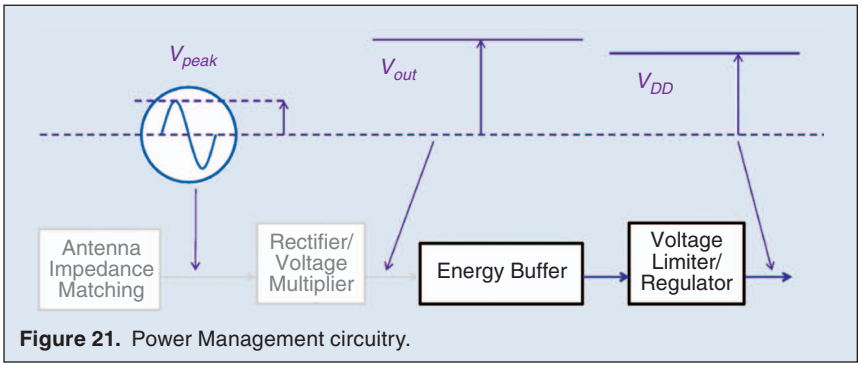


Figure 21. Power Management circuitry.

the harvester output, removing ripple voltages caused by the rectifier's nonlinear operation [78]; since practically every rectifier contains a capacitor in the final stage for this task, even circuits without a "dedicated" buffer component can be said to contain some buffering. Larger buffers can also be implemented with capacitors [14], [43], though very large capacitances such as supercapacitors may require additional charging time and digital overhead that only charges the element when there is an excess of available power [87], [88]. The largest buffers can be implemented with a small rechargeable battery [46], which grants extensive power storage at the cost of a larger circuit size and higher cost [89]. Passive circuits with this scale of buffer can often capitalize on range and efficiency in the rectifier design, as losses in efficiency can be compensated for by using a long pre-charging period, gradually building the energy required to perform the intended task [45].

The voltage limiter is a no less essential component used to keep harvester output voltages in check, and prevent excessive power levels from damaging the delicate elements in the low power digital back-end. Many of the applications for RF embedded systems will involve variable ranges, especially those used in supply chain tracking or consumer applications, where the same chip will be expected to be operational at any range between 1 m and 10 m. At close range, the voltage available at the output of the rectifier may spike to levels that could damage or destroy the components it is intended to power: to prevent this from happening, a voltage limiter must be introduced to place a hard cap on the allowed voltage level and short any voltage exceeding that to ground. This voltage limiter is usually as simple as a zener diode or MOS configuration engineered to maintain a stable voltage level during power surges. Some designers may opt to go beyond the use of limiters and implement a full voltage regulator, which will step voltage up or down to maintain the desired value at the IC input. However, the more complex the design of the regulator, the more energy will be expended [90]. Thus, out of concern for efficiency, most far field applications have opted for the simplest possible limiter designs, assuming that the real area of efficiency is the region of lowest power, and that operation at voltages higher than that is of secondary concern.

B. Load Resistance

Another task that may be implemented at the output of the harvester unit is dynamic resistive matching. While the input impedance seen at the rectifier input is transformed and altered by the structure and stage number, its resistive value is still a function of the load resistance at the output R_L. When activated, circuit limiters may draw a substantial amount of current [42], altering the impedance equivalent of the back-end and potentially disrupting the impedance matching network at the antenna. Since most circuits will achieve their best power transfer for a specific constant resistance, computational control over current draw via a digital logic system may be necessary to preserve PCE for a wide range of input power. In active systems, *Peak Power Tracking* (PPT) can be performed through a variety of digital methodologies, but under the stringent power constraints of passive systems only a few methods remain viable [91]. These strategies, which include adapted traditional power stepping techniques at microscale technologies, have been briefly explored but not widely seen in existing wireless power harvesting technologies. PPT is highly related to the Maximum Power Point Tracking (MPPT) methods widely used in solar energy harvesting [92], [93], which modulate the load resistance imposed on the solar panels to achieve peak power output from solar panels that have a nonlinear Voltage-Power curve.

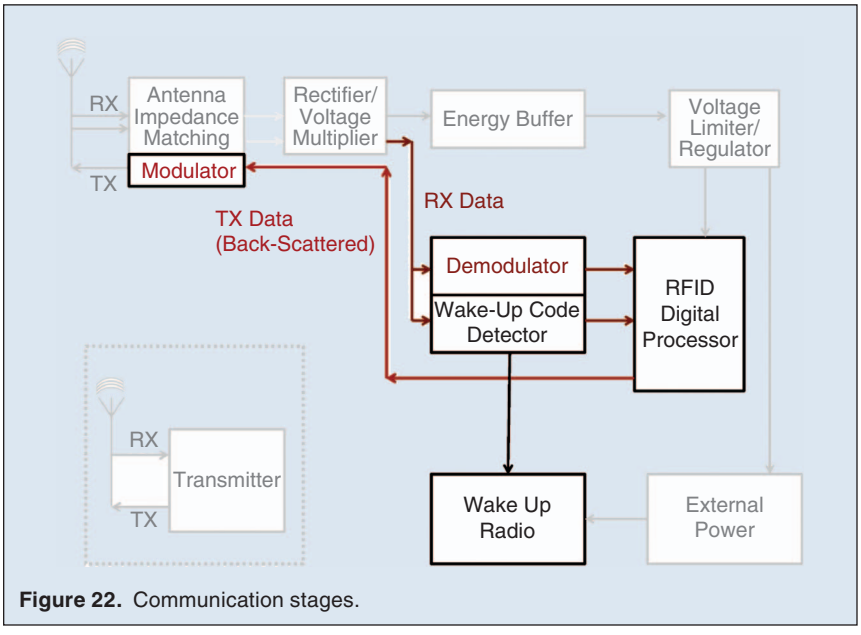


Figure 22. Communication stages.

C. Dedicated-Source Power Harvesting

For certain circuits, such as those used for ambient harvesting, or those used to power a sensor node that has no use for backscattered communication, the sole purpose of the digital back-end is to maximize the energy taken in by the harvester and store it for future

use. In these cases, signal properties such as ripple voltage or instability are of no real concern, since the IC is not dependent upon them for voltage, clock reference, or a backscatter carrier [89]. For these cases, certain shortcuts may be taken during design of the power management. For circuits harvesting from a dedicated transmitter, more extreme versions of the Power Optimized Waveforms discussed in Section IV-D may be used without penalty, maximizing the peak voltage in the absence of concern for ripple interference or harmonic signal distortion [33]. Circuits performing ambient harvesting will be unable to use POW optimization, as their designers usually have no control over the signals transmitted by distant commercial broadcast towers. However, ambient harvesting units may have more flexibility in the design of their buffering storage units, as device turn-on time is no longer a limiting factor on the selection of capacitive charging elements. Other improvements may also be available depending on location, application, and the nature of the circuit requiring harvested energy.

D. Design Examples: Power Management

Example: Karthaus [14] describes a passive RFID IC with an input power of $P_{RFin} = 12.5\,\mu$W. After rectification, this rectifier provides a $V_{DD} = 1.5$ V and $I_{DD} = 1.5\,\mu$A to the digital part of the IC. Power conversion efficiency (PCE) for this configuration is 18%, since only $2.25\,\mu$W out of the incident $12.5\,\mu$W has been turned into useful power.

Example: Paing et al. [90] investigate a design using discrete components, such as BAT43WS Schottky diodes and Si1568EDH N Channel MOSFET transistors. They emulate the load resistance by modulating the PWM duty cycle of a buck/boost converter built out of BAT43WS and Si1568EDH. Their goal is to harvest as much power as possible using the Maximum Power Tracking method. Since the buck/boost converter requires power in the mid-μW range just to operate, their circuit only works with a $P_{RFin} =$ 50–500 μW. These input power levels are at the very high end of an RFID transceiver circuit, thereby making the RFID circuit highly efficient. They report a PCE = 65%, which is substantially higher than the previous example which reports PCE = 18% @ $P_{RFin} = 12.5\,\mu$W. Additionally, at $P_{RFin} =$ 50–500 μW, [90] reports a $V_{DD} =$ 3.3 V, which is sufficient to power a microcontroller such as a PIC that stores the excess energy into a supercapacitor [92].

Example: Paing et al. [91] report results on an IC integrated using a $0.35\,\mu$m CMOS technology which incorporates a Boost converter. Their test results at an operating frequency of 1.93 GHz and $P_{RFin} =$ 1.5–30 μW show PCE = 35–70%. Their IC works by emulating the RF harvesting resistance to match the incoming RF power. This implies that, a portion of the harvested energy might not be immediately used as it is harvested. Therefore, a buffering mechanism is required. In [91], the authors suggest the use of a microbattery for energy buffering. Harvested output voltages are sufficient to power up a microcontroller-operated harvester such as [93].

X. Analysis: Communications

For many of the applications of RF power harvesting, the incoming RF waveform is not only used for power, but also for communication and data transmission. This communication may be periodic or constant, activate immediately or after a charging delay, and may use any number of different modulation and encoding types to transmit binary data. Tags may also use the incoming signal as a carrier wave for *reflective backscatter*, allowing for two-way communication with a reader device. Since all of these forms of communication alter the incoming waveform in some way, they inevitably have an effect on the efficiency and sensitivity of the harvester circuit. To assist in the design of high-value harvester circuitry, a brief summary of communication types and technologies has been assembled, along with their pros and cons between different potential applications.

Almost every form of communicating passive chip falls under the label RFID. While there are some technologies that perform communication tasks outside this field, these devices inevitably use nearly identical technology for the communication components, and can be addressed using the same terminology and even the same overall circuit structure. Typical communication units in an RFID chip are 1) *demodulator/modulator*, 2) *oscillator*, 3) *Power On Reset* (POR), and 4) *digital back end*.

A. Demodulation and Modulation

At the terminals of the antenna of an RFID device, usually connected in parallel to the power harvester unit, are the *modulation* and *demodulation* units for interpretation and encoding of waveform data. Depending upon the modulation scheme, the structure of these units will vary considerably. Demodulators for amplitude communication often mimic a single stage of the rectifiers mentioned in Section VIII, collecting voltage data from the DC envelope while drawing as little power as possible away from the multiplier. Conversely, demodulation for phase or frequency based communication types may include integrators and clock units to interpret data from time delays in the signal. Modulation units are similarly variable, using reconfigurable connections to alter the impedance of the matching network depending on the needs of the backscatter type. A modulation component must be designed around one or more modulation types, which have a number of tradeoffs regarding their efficiency, consistency, and communication error rates as discussed later in this section.

B. Wake-Up and Interpretation

Another critical decision made by communications circuits is how to initiate and coordinate the different stages of transmission. Units such as the *Power On Reset* and *Oscillator Clock* unit may be used for this purpose. The POR is used to activate the digital processing and networking elements once the power received by the harvester has reached a sufficient point, clearing all outdated memory and initiating a new communications session. Conversely, the clock unit dictates the period and synchronization of the communications session, often coordinating to the period of the incoming signal to ensure correct decoding and a non-conflicting backscatter process. It is critical that these elements be tuned to ensure maximum efficiency - a circuit that turns on too quickly may expend all available energy resources before it has finished communicating, and a carefully designed timing network may preserve extra power by duty cycling operations and minimizing communication errors. The exact technological specifics for the construction of these elements varies widely between applications and is well outside the scope of this paper; however, note that in some application cases such as those discussed in Section XI, similar designs to the RFID POR can be implemented in circuits that have no backscatter component to turn on a larger, non-passive circuit interface.

C. Modulation Through Backscattering

One of the many critical considerations in the design of a communicating chip is the modulation type and its supporting hardware, as the manufacture of these components will directly affect the performance of the rectifier and matching element, altering the amount of energy being harvested at any given time. All communication comes at the cost of some efficiency in the rectification. As the waveform assumes different states through amplitude or phase to encode high and low bits, the matching network and rectifier will no longer reach full efficiency for one or both stages, and some energy will be lost through reflective and resistive losses. In the case of backscatter, these changes may actually be intended, but in order to maintain adequate circuit power it is essential that these communication losses be balanced with the required harvested power.

While a transceiver communicates by means of a received signal and a transmitted signal, these RX and TX activities require on the order of multiple 10 mW operating power levels, depending on the required transmission power levels. Such power consumption levels are feasible for active tags operating from a battery, but not for passive devices with sub-100 μW power budgets. The backscattering mechanism that allows such low operating power levels has its roots in the groundbreaking 1948 paper by Stockman [94]. As discussed previously in Section VII, a perfectly matched antenna in the impedance matching stage of a receiver will incur no reflective losses (i.e., $\Gamma = 0$), absorbing 100% of the incident power at the antenna. Alternatively, a mismatched antenna causes a high reflection (e.g., $\Gamma = \mp 1$ in the case of complete mismatch). In [94], Stockman describes how the mismatch can be caused intentionally as a means to communicate with the transmitter. Since the transmitter receives RF power proportional to the reflected waveform, the "0" and "1" bits of the communicated message can be produced by means of load modulation at the receiver, by varying Γ.

D. Modulation Types

Different modulation types are shown in Fig. 23. This figure depicts the circuit implementation (left), corresponding waveform (middle) and the resulting reflection coefficients (right) for different types of modulation.

Amplitude Shift Keying (ASK): Amplitude Shift Keying utilizes a change in the resistive component of the circuit impedance to alter the amplitude of the carrier signal, as shown in the waveform of Fig. 23a. This is typically implemented by inserting a resistor into the matching network or load [10], altering the structure of the multiplier to change its input resistivity, or by altering the step rate of a backend voltage regulator [28]. ASK signals are simple to both modulate and demodulate, and require little additional circuitry to implement as return backscatter; thus, ASK has become one of the most commonly used forms of communication for RFID in both reader and tag designs. However, amplitude based communication is susceptible to noise and external signal interference, and the implementation of the resistor will cause persistent power losses in addition to the reflected signal loss at the antenna, decreasing viability for many applications [14]. Figure 23a depicts an example of ASK on a Smith Chart with triangle symbols, corresponding to $\Gamma = 0.5$ and $\Gamma = -0.5$ for sending "0" and "1" bits. Note that, in this specific case, there is a power loss in each state, but, there is also harvested power in each state, and the IC is never starved of harvested power.

On Off Keying (OOK): Considered to be an extreme form of ASK (and occasionally labeled as such), OOK is distinguished from the other modulation types by not using two symmetrical states with identical power performance as shown in Fig. 23b. Instead, On Off Keying switches between an optimally matched condition (On) and a total mismatch condition (Off). These two conditions correspond to the two circles on the Smith Chart shown in Fig. 23b. The On state is characterized by no reflection, i.e., $\Gamma = 0$, as indicated by the circle at the center of the Smith Chart. On the other hand, the Off state is characterized by 100% reflection, i.e., $\Gamma = 1$, as indicated by the circle at the right edge of the Smith Chart. The circuit receives power only during the On state, foregoing all harvesting potential when reflecting 100% during the Off state. OOK is implemented

in hardware by either shorting or opening the antenna terminals, the former case of which is shown on the left side of Fig. 23b. To prevent loss of functionality while communicating, OOK requires a power buffer (typically a capacitor) to maintain a sufficient IC voltage while backscattering, and will additionally benefit from non-direct encoding types such as Manchester that maintain stable average power. However, the total match condition during the On state dictates that OOK will have a higher peak voltage than other modulation types, which will have a consistently depressed input power during both phases of communication. Besides providing superior performance at the rectifier, the heightened contrast between phases also results in a much lower Bit Error Rate than other modulation types. For these reasons, OOK is widely used for backscatter modulation, despite an overall efficiency disadvantage in comparison to other modulation schemes.

Phase Shift Keying (PSK): An alternative to the real-impedance keying of ASK and OOK, mismatch is used to implement Phase Shift Keying. PSK utilizes a reactive element (usually a capacitor) in series or parallel to the matching element, causing a mismatch in the reactive impedance that results in a certain proportion of the power being reflected at the antenna. This reflection manifests itself as a phase shift in the carrier wave as shown in Fig. 23c, which can be detected by the reader as a form of communication. PSK backscatter systems are simple to implement in tag hardware, although they are more complicated to demodulate and are typically not used for the reader-to-tag communication. Due to their consistent transmission power envelope, PSK signals are not nearly as vulnerable to external signals as ASK, and can utilize higher data rates for similar results in BER and SNR. For these reasons, several RFID publications have recommended the use of PSK communication over the amplitude based ASK and OOK modulation types [14].

Frequency Shift Keying (FSK): The final form of modulation is Frequency Shift Keying, as shown in Fig. 23d. FSK is typically implemented through alteration of pulse width in a square wave ASK signal, rather than modulation of the base frequency, and for this reason has occasionally been referred to as Pulse Width Modulation (PWM) signaling [14]. The modulation is not characterized by a change in impedance, unlike the other forms of backscatter communication, and thus cannot be visualized on a Smith chart or characterized using the same equations. FSK backscatter signals have lower susceptibility to interfering signals and

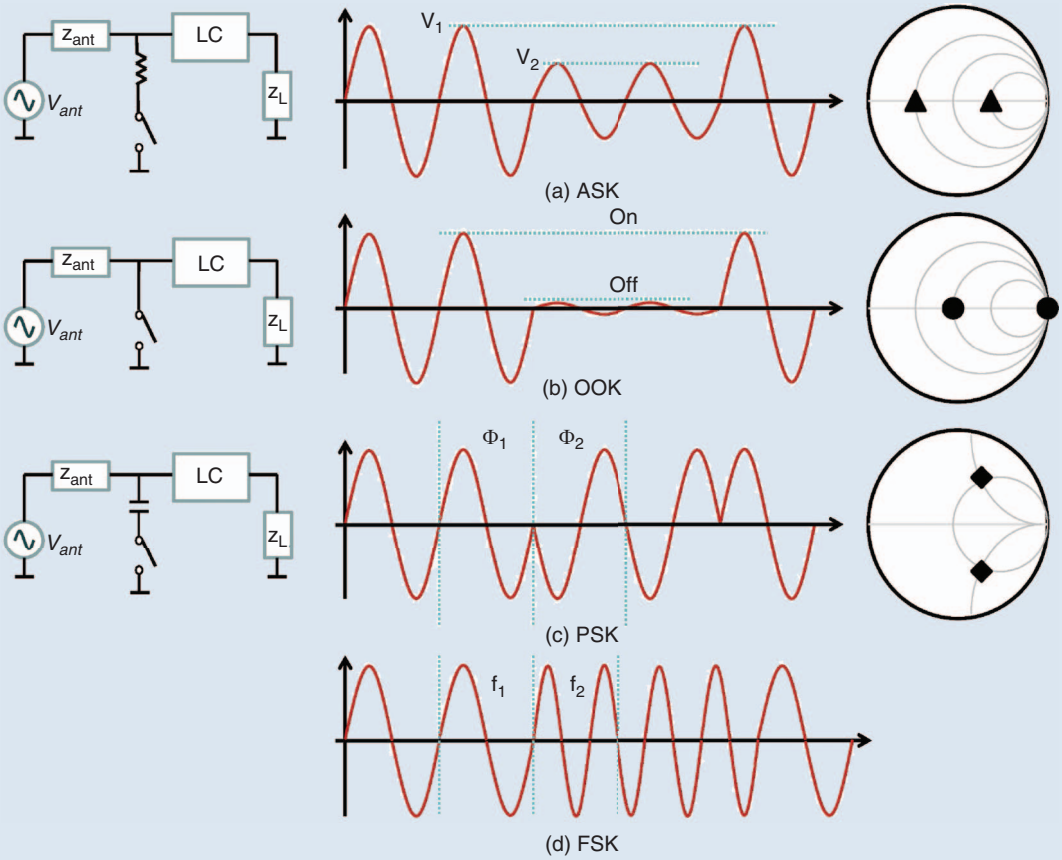


Figure 23. Different modulation standards and their operation plotted on Smith Chart.

noise than PSK, and have lead to widespread use in passive RFID, even being standardized as a generational standard for reader-to-tag communication [77]. However, at extreme far field, the more sophisticated modulation hardware makes FSK impractical for backscattered tag-to-reader communication. Some tags may also rely on the carrier wave for a synchronized clock, a process that is hampered by the pulse-altering methodology of the FSK data stream. These drawbacks, along with FSKs more demanding and legally restricted bandwidth requirements, can outweigh the method's advantages when selecting between alternative forms of two-way communication.

E. Harvesting/Communication Tradeoffs of Modulation

Since each modulation type trades off *power harvesting efficiency* for *communication efficiency*, two corresponding metrics can be defined to quantify these: First, the quality of the backscattering communication depends on the distance between the "0" and "1" points on the Smith Chart. The farther apart they are, the easier it will be for the reader to distinguish between the A and B states (i.e., "0" bit vs. "1" bit). This can be quantified as follows [95]:

$$M_C = \frac{1}{4}|\Gamma_A - \Gamma_B|^2 \tag{21}$$

where Γ_A and Γ_B are the reflection coefficients (from Eq. 13) for the A and B states, and M_C is the *Communication Modulation Efficiency*. Increasing M_C increases the *Signal to Noise Ratio* (SNR) and lowers the *Bit Error Rate* (BER) at the transmitter due to the deeper (i.e., more efficient) modulation, i.e., much more pronounced amplitude/phase differences between the A and B states. Therefore, the design goal is to increase M_C as much as possible. In Eq. 21, M_C quantifies the relative percentage compared to the maximum theorecially achievable modulation depth. $M_C = 1$ (i.e., 100% modulation depth) denotes the extreme case where the two states are on the opposite ends of the unit circle of the Smith Chart and their distance is 2. An example of such a case is achieved when $\Gamma_A = 1$ and $\Gamma_B = -1$. In this case, since all of the power is reflected in both states, the RFID tag is completely starved of any harvested power, which is clearly not an acceptable option. Thus $M_C = 1$ is not a practical option.

Second, we define a metric that quantifies the power harvesting efficiency. To formulate this metric, we call upon the Smith Chart analysis again. Noting that the middle circle on the Smith Chart represents 100% power efficiency (i.e., $\Gamma = 0$), the farther each state is from this point, the less efficient the power harvesting is. For each state, the power reflection (i.e., power loss) is $|\Gamma|^2$ according to Eq. 14, thus, the power efficiency is $(1-|\Gamma|^2)$. Averaging the power efficiency in both states, we get:

$$M_P = 1 - \left(\frac{|\Gamma_A|^2 + |\Gamma_B|^2}{2}\right) \tag{22}$$

where M_P is the *Power Modulation Efficiency*, and Γ_A, Γ_B are the state reflection coefficients as defined previously. M_P is also defined relative to the maximum theoretically achievable efficiency, where $M_P = 1$ denotes the impractical extreme case where all of the incident power is harvested, leaving no power for communication.

We will define a third metric as follows:

$$M_{Pc} = \frac{\min\left(1 - |\Gamma_{A,B}|^2\right)}{\max\left(1 - |\Gamma_{A,B}|^2\right)} \tag{23}$$

where M_{Pc} is the *Power Modulation Consistency*. This metric is also relative to its maximum achievable 100% rate. $M_{Pc} = 1$ denotes the best power consistency case, where the harvested power is identical in both states, whereas $M_{Pc} = 0$ denotes the worst power consistency case, where there is no power in one case (e.g., OOK).

Based on these three definitions, Table 3 provides example cases for different modulation types. Note that, for simplicity, the duty cycle of each state is assumed to be equal at 50%. In [14], Karthaus introduces d_A and d_B, which are the duty cycles for states A and B. In a system where these duty cycles are asymmetric, this can be easily incorporated into Eq. 22 by replacing $|\Gamma_{A,B}|^2/2$ with $d_{A,B}|\Gamma_{A,B}|^2$. Similarly, Eq. 23 can be generalized by replacing $|\Gamma_{A,B}|^2$ with $d_{A,B}|\Gamma_{A,B}|^2$.

F. Design Examples: Communication

Example: Karthaus et al. [14] provide an analysis of the tradeoffs between ASK and PSK. They conclude that, OOK is widely used in 125 KHz and 13.56 MHz RFID circuits and ASK is more popular at higher frequencies due to its better power consistency. Their implementation uses PSK by modulating the capacitance of an accumulation-mode MOS varactor (variable capacitor). Modulating the capacitance modulates the imaginary part of Γ, similar to the circuit shown in Fig. 23c. The capacitor is implemented in a $0.5\,\mu$m CMOS technology and its capacitance is modulated by changing its gate voltage via the switch shown in Fig. 23c. This switch is also implemented by multiple MOS transistors that receive their logic input from the digital modulator circuitry.

PSK was used in [14] with $\Gamma_{A,B} = 0 \pm 0.41j$ (pure imaginary reflection $|\Gamma| = mj = (\sqrt{2} - 1)j = 0.41j$ in both A and B states). Therefore, $|\Gamma_A|^2 = |\Gamma_B|^2 = 0.17$. According to Eq. 21, Eq. 22, and Eq. 23, we compute $M_C = 0.17$, $M_P = 0.83$, and $M_{Pc} = 1.0$, respectively. These results, also repeated in Table 3, demonstrate a symmetric PSK implementation that favors power over communications,

and has an excellent power consistency. Compared to a symmetric ASK implementation shown at the top of Table 3, the reduction in modulation depth is not substantial (i.e., 17% instead of 25%). However, the power efficiency is improved noticeably from 50% to 83%, thereby potentially improving the sensitivity, and hence, the operating distance of the RFID circuit. On the other hand, the disadvantage of this PSK implementation is the added complexity to the design of the IC.

Example: Yao and Hsia [96] describe a dual-channel IC that receives its RF power from a 866–925 MHz "uplink" and uses the same channel for backscattering. It receives its "downlink" data from a second 433 MHz band, which provides a 15b ID to the chip. If the built-in ID of the chip matches this transmitted ID, the chip activates and sends a response through the uplink using backscattering FM0 modulation. The chip ID is sent by the transmitter through the downlink using ASK, and more specifically using Pulse Interval Encoding (PIE).

In PIE, a *Tari* is defined as the unit of transmission time for data bits. Typical Tari values are 6.25 μs, 12.5 μs, 25 μs, permitting symbol rates of 160 kbps, 80 kbps, and 40 kbps [28]. PIE defines a "0" transmission as a (1/2) Tari period HIGH (H) followed by a (1/2) Tari period LOW (L) using ASK. A "1" bit is transmitted by sending a 1.5–2 Tari period H followed by a (1/2) Tari period L. These H and L symbols are transmitted using high-maplitude and low-amplitude ASK-modulated waves at the same exact frequency (e.g., 915 MHz).

The IC in [96] uses an FM0 modulation to communicate back to the transmitter via ASK backscattering. In FM0 modulation, a LOW (L) and a HIGH (H) state is needed, which are implemented by an NMOS transistor shorting the antenna (L) or leaving the NMOS open-circuited (H). The response data bits are then sent as combinations of the L and H states as follows: HLHL and LHLH denote 00, whereas HLHH or LHLL denote 01. Similarly, 10 is transmitted by either HHLH or LLHL, and 11 is transmitted by either HHLL or LLHH. This encoding (and, hence the IC implementation in [96]) then achieves OOK-like metrics, where no power is generated when transmitting an "L" and 100% power is harvested when transmitting an "H".

XI. Comparative Tradeoffs

Table 4 describes the genres of design change for power harvesting circuits and relates them to the critical tradeoffs that must be considered when making design decisions for that focus and its associated figures of merit. The stage of the circuit with the most effect on this design focus is also linked: for example, when considering the number of rectifier stages, tradeoffs exist between efficiency and sensitivity, as well as efficiency and multiplication, where maximizing one may lead to the degradation of the other. These changes would be implemented in the Rectifier/Voltage Multiplier stage of the circuit. Let us now briefly go through Table 4 by focusing on each design stage.

Design/Transmission: As a general comment, one of the biggest challenges in RFID circuit design is the handling of the extremely low RF input voltages, typically less than 100 mV. Manipulating the operational *frequency* or *transmission power* would alleviate these problems partially, however, regulatory restrictions allow operation

Table 3.
Example modulation cases and their implied tradeoffs in communication efficiency (M_C, Eq. 21), power efficiency (M_P, Eq. 22), and power consistency (M_{Pc}, Eq. 23). All of these terms are defined relative to their maximum achievable value of 100% (i.e., 1.0). Due to the implied tradeoffs among these metrics, achieving 100% is not practical for any of them, as this would imply 0% on one of the other metrics.

Modulation	Γ_A	Γ_B	M_C	M_P	M_{Pc}	Notes
ASK	0.5	-0.5	0.25	0.50	1.0	Symmetric ASK. Fig. 23a
ASK	0.3	-0.5	0.17	0.83	0.82	Asymmetric ASK favoring power over communications
ASK	0.8	-0.5	0.42	0.55	0.48	Asymmetric ASK favoring communications over power
OOK	0.0	1.0	0.25	0.50	0	Fig. 23b. State B=short
OOK	0.0	-1.0	0.25	0.50	0	Same as Fig. 23b, but State B=Open circuit
PSK	0 + 0.41 j	0 - 0.41 j	0.17	0.83	1.0	Karthaus [14]. Modulate Im (Γ) with a varactor
PSK	0.5 + 0.5 j	0.5 - 0.5 j	0.25	0.50	1.0	Fig. 23c using resistive and capacitive modulation
PSK	0.5 + 0.7 j	-0.3 - 0.9 j	0.80	0.18	0.82	Asymmetric PSK favoring communications

only within very well defined regions, such as a maximum P_{EIRP} of 4 W and ISM band frequencies of 915 MHz, etc. Manipulating the shape of the transmitted waveform through *Power Optimized Waveforms* is possible, albeit at reduced bandwidth or Peak Substage Voltages. Alternatively, to improve the consistency of the received power, *Special encoding* techniques, such as FM0 or PIE can be utilized, but they reduce the data rate due to the built-in redundancy in their definition. These tradeoffs appear as the very first few lines in Table 4.

Antenna Impedance Matching: Dealing with very low RF input voltages has the highest impact on the rest of Table 4 in terms of the other tradeoffs that must be considered to achieve optimum operating conditions. Firstly, since the RF input voltage is lower than the voltage drop of Schottky diodes (e.g., 200 mV) or the threshold voltage of a typical NMOS transistor (e.g., 220–300 mV), much of the design efforts have focused on obtaining some sort of voltage boost right at the LC matching circuit, since this stage is built out of low-voltage-friendly inductors and capacitors, rather than semiconductors with inherent voltage barriers. These tradeoffs are shown in the rows pertaining to the *Antenna Impedance Matching* stage in Table 4. No solution is perfect, since adding more LC components will increase the size of the circuit due to the large relative size of the inductors and capacitors within the IC, as exemplified in Section VIII-E. Additionally, these LC components introduce parasitic RLC components, which degrade the overall circuit performance. Despite the great appeal of voltage boosting, the maximum attainable boost ratios are limited by the antenna resistance, load resistance/capacitance of the IC and the parasitic values of the RLC components within the IC design. Typical values of 3–8 have been reported by many researchers.

Table 4.
Comparison of the tradeoffs in different design stages. The notation Range/Size means "Range vs. Size."

Design Focus	Tradeoffs	Stage
Frequency	Range/Size	Design
	Efficiency/Legal	
Transmission Power	Power/Legal	Design
Power Optimized	V_{peak}/BER	Transmission
Waveforms (POWs)	Efficiency/Bandwidth	
Special Encoding	Reliability/Bandwidth	Transmission
Antenna	Efficiency/Complexity	Antenna Imp.
Optimization	Sensitivity/ Size	Matching
	V_{peak}/Complexity	Antenna
Matching Type	Efficiency/Cost	Impedance
	Efficiency/Size	Matching
LC Boosting	V_{peak}/Reliability	Antenna
	V_{peak}/Cost	ImpMatch
	Sensitivity/Size	Rectifier/
Rectifier	Efficiency/Cost	Voltage
Structure	Reliability/Cost	Multiplier
	Efficiency/Complexity	
Number of	Efficiency/Sensitivity	Rectifier/
rectifier stages	Efficiency/Multiplication	Voltage Mult.
Diodes vs.	Sensitivity/Cost	Rectifier/
Transistors	Sensitivity/Size	Voltage
	Sensitivity/Reliability	Multiplier
Buffer	Reliability/Size	Power
Selection	Complexity/Efficiency	Management
Limiter/	Reliability/Efficiency	Power
Regulator	Efficiency/Avail.Voltage	Management
	Efficiency/Cost	
Modulation/	Complexity/Functionality	Communications
Demodulation	Complexity/Efficiency	
Modulation	V_{peak}/Complexity	
Type	V_{peak}/Cost	Communications
	V_{peak}/BER	

Rectifier/Voltage Multipier: The LC boosting can be thought of as being "passive voltage bosting", whereas the rectifier circuit achieves its "active voltage boosting" by using multiple rectifier stages that incorporate Schottky diodes or diode-connected MOS transistors. Voltage multiplication is achieved by N cascaded stages of charge pumps, connected in one of the few popular topologies such as Dickson, Greinacher, etc. N cannot be increased arbitrarily, since each added stage, despite performing further voltage multiplication, introduces additional parasitic capacitances and voltage drops in the Schottky or diode-connected MOS transistors. These tradeoffs place optimum N values at around 3–6 for many designs, although, other designs with much higher stages have been reported as we will see in Section XII.

Power Management: The tradeoffs related to the power management stage of the RF circuit change substantially based on whether there is a continuous supply of RF power vs. the power has to be buffered due to unexpected interruptions in the supply. Certain designs suggest the use of supercapacitors or microbatteries for buffering purposes. In general, a typical RFID chip expects the RF power to be available every cycle to assure a continuous operation. Only extremely minimal buffering (a few RF cycles) can be performed with internal bypass capacitors within an IC, since the capacitors occupy

a substantial IC die area. These tradeoffs are listed towards the end of Table 4.

Communications: The modulator part of the RF circuit, and the utilized modulation type have a dramatic effect on the power supply of the circuit due to the way backscattering works. Without losing power, there is no way to transmit-back a message to the receiver. This presents possibly the most important tradeoff in RFID circuit design in that, an IC that favors communication quality will harvest less RF power, or vice versa. Some example tradeoffs were listed previously in Table 3.

XII. Conclusions and Future Work

Table 5 summarizes the passive RFID transponder design efforts within the time period of 2003-2014, when passive RFID enjoyed strong research activity. These efforts simply comtemplated the tradeoffs summarized in Table 4 and made different design choices based on these tradeoffs. The choice of the tradeoffs depends on the RFID architecture as well as the CMOS technology that is being used. For example, some designs used circuit components such as FeRAM or Schottky diodes that are not compatible with standard CMOS processes, thereby making the manufacturing more expensive.

Table 5.
Comparison of the existing work in the literature. SOS=Silicon on Sapphire.

Source	Year	Freq (MHz)	Pin (dBm)	PCE (η_c)	V_{DD}	Rectifier {# stages}	CMOS Technology	Notes
Karthaus [14]	2003	868–915	-17.78	18%	1.5 V	Dickson {4+}	0.5 μm	Schottky, EEPROM
Curty [42]	2005	915	-18	$<$ 10%	2 V	Greinacher {3}	0.5 μm SOS	Dynamic Model
Curty [46]	2005	2450	-25.7	37%	0.882 V	Mirrored {3}	0.5 μm SOS	μPower rectifier model
Umeda [97]	2006	950	-14 (-6)	1.2–11%	1.2 V	Dickson {6}	0.3 μm	Battery charging
Paing [90]	2006	RF	-5 (+2)	65%	3.3 V	Buck/boost	discrete	Resistor emulation (sim)
Tran [73]	2007	900	-22.22	45%	1.5 V	Dickson {6}	0.35 μm	Schottky, LC matched
Nakamoto [65]	2007	950	-6	36.6%	3 V	Mirror stack {1}	0.35 μm	FeRAM
Yi [70]	2007	900	-11.12	26.5%	1 V	Dickson {24}	0.18 μm	Very low V_{TH} MOS
Mandal [79]	2007	970	-22.22	16.7%	0.4 V	DiffDrive {3}	0.18 μm	Not biased
Bergeret [76]	2007	900	-11.82	$<$ 6.3%	1.2 V	Dickson {3}	0.18 μm	EEPROM
Shameli [52]	2007	920	-14.1	5%	1 V	Dickson {4}	0.18 μm	LC Boosting
Ma [98]	2008	902–928	-16.78	31.9%	1.8 V	Mirror stack {3}	0.18 μm	High Vin. No antenna match.
Le [43]	2008	915	-22.6	8.5%	1.3 V	{36}	0.25 μm	44 m for $P_{EIRP} = 4$W
Yao [99]	2009	900	-19.25	18.56%	1.5 V	Dickson {9}	0.35 μm	$V_{TH} = = 0$ MOS transistors
Paing [91]	2009	1930	-19 (-6)	35–70%	2.5–4.15 V	Boost	0.35 μm	MPP: store into μ battery
Lee [100]	2009	900	-14.8	36.2%	1.5 V	Dickson {5}	0.35 μm	16b ID. Ti-Si Schottky. ASK
Baghaei [101]	2009	900	-18.5	29%	2.75 V	{7}	0.18 μm	I-UWB Uplink=3.1–10.6 GHz
Soltani [51]	2010	2400	-11 (-2)	15–30%	1.8 V	Mirrored {1}	0.18 μm	Transformer matched
Wong [80]	2011	915	-13.41	74%	1 V	DiffDrive {3}	90 nm	Optimized biasing, sim
Marian [48]	2011	2450	-20	$<$ 25%	$<$ 0.5 mV	Rectenna {1}	discrete	Uses discrete components
Papotto [60]	2011	915	-24	11%	1.2 V	{17}	90 nm	Harvester: RF sensors networks
Scorcioni [81]	2013	840–975	-16	60%	2 V	Par Cross Coup.	130 nm	Dynamic impedance matching
Mansano [86]	2013	13.56,915	-20 (-6)	2–8%	1–5 V	Simulated 3–9	0.18 μm HV	Simulation: 90 nm IBM9RF
Yao [96]	2014	866–925	-21.2	43%	0.84–1.32 V	Dickson {8}	0.18 μm	Downlink = 433 MHz. FM0, PIE

Table 6.
List of abbreviations used in this survey along with related citations and section references.

Term	Meaning	Section	Description
IoT	Internet of Things	I	An internet-connected network of self-addressable devices
UHF	Ultra High Frequency	I	The 300 MHz–3 GHz frequency band
RFID	Radio Frequency Identification	III-A	1–100 μW devices capable of performing dedicated simple tasks
WSN	Wireless Sensor Networks	III-B	A connected network of active sensors, operating typically within the UHF band
WUR	Wake-up Radio	III-B	A dedicated passive RF device to detect an ID and wake-up an active WSN device
WiFi	Wireless Fidelity	III-B	A widely used communication protocol, standardized by IEEE 802.11x
λ	λ=Signal Wavelength	IV-B	The distance during which an RF wave completes one cycle period.
ISM	Industrial-Scientific-Medical	IV-B	open bands covering the 915 MHz and 2.4 GHz
EIRP	Equivalent Isotropically Radiated Power	IV-C	mention that, legal limit is 4 W in the US.
POW	Power Optimized Waveforms	IV-D	Non-standard waveforms to induce higher voltages at the receiver
ESA	Electrically Small Antenna	IV-D, VII-G	An antenna with its largest dimension less than λ/10
FoM	Figure of Merit	VI	A numerical expression to quantify a property of a device (e.g., efficiency)
PCE	Power Conversion Efficieincy	VI-A	% of the absorbed RF power converted to useful power (Eq. 5)
dBm	DeciBel-milliWatts	VI-B	A logarithmic scale to quantify power, as per Eq. 6
V_{peak}	Peak Passive Voltage	VI-C	Peak amplitude of the sine wave at the rectifier input (LC matching output).
Q	Quality Factor		Q is the reactance/resistance for inductors, i.e., the "useful" impedance
Γ	Γ=Reflection Coefficient	VII-A	Γ is the Voltage reflection coefficient, based on Eq. 13
$\lvert\Gamma\rvert^2$	$\lvert\Gamma\rvert^2$=Power Ref. Coeff.		whereas $\lvert\Gamma\rvert^2$ is the power reflection coeff. based on Eq. 14
IVC	Internal Voltage Cancellation	VIII-C	An IC design technique to de-sensitize the circuit to V_{TH} thresholds
PPT	Peak Power Tracking	IX-B	Modulating the load resistance to reach maximum harvested power [91]
POR	Power On Reset	X	An IC performs this internal reset when it reaches a sufficient RF input level
BER	Bit Error Rate	X-C	Number of incorrect bits per unit time. Lower is better.
SNR	Signal to Noise Ratio	X-C	Ratio of the signal amplitude relative to the available noise
ASK	Amplitude Shift Keying		ASK modulates the wave amplitude, e.g., H=high amplitude, L=low amplitude
OOK	OOK Shift Keying		OOK is an extreme case of ASK, where H=full amplitude, L=zero amplitude
PSK	Phase Shift Keying	X-D	PSK modulates the phase of the wave, e.g., L=zero phase, H=180° phase
FSK	Frequency Shift Keying		FSK modulates frequency, L=f1 and H=f2, i.e., two different frequencies
FM0	FM0 Encoding	X-F	An encoding, where 0={LH or HL} and 1={HH or LL}. L and H are symbols.
PIE	Pulse Interval Encoding	X-F	00=HLHL, 01=HLHH, 10=HHLH, 11=HHLL or replace H's with L's completely

Alternatively, lower technology nodes (e.g., 90 nm) can realize lower inductance and capacitance values and might have lower relative parasitic RLC values, and lower MOS transistor threshold voltages, thereby making the design more robust. However, these technology nodes are typically more expensive to use for manufacturing the RFID chips.

The common denominator in every design is dealing with the ultra-low voltages that are indicent at the receiver antenna. Since the incident voltage at the RF antenna is much lower than the threshold voltages of active devices such as MOS transistors or Schottky diodes, this necessitates a system architecture where the LC matching is also responsible for partial voltage boosting. However, the amount of the voltage boost is limited by the parasitics of the RLC devices being used in the circuit. The matching circuitry is connected to a charge pump circuit, made up of multiple stages, each stage multiplying the voltage, however, causing a voltage drop that is equal to the threshold of either the Schottky diodes or the NMOS transistors. Some of the designs suggest techniques to cancel out the voltage drops through Internal Voltage Cancellation (IVC). Due to the added parasitic capacitance of the active elements in the charge pumps, the number of rectifier stages cannot be arbitrarily increased as evidenced by Table 4, where most designs stay within the range of 3–8 stages.

Although a typical passive RFID design harvests its energy cycle by cycle and does not buffer the excess energy (if any), some designs suggested the use of small μbatteries or supercapacitors to eliminate the loss of power during intermittent transients. The choice of the modulation/demodulation type was not necessarily emphasized in these designs, but ASK, OOK, and PSK are the common ones due to the simplicity in implementing them. The choice of the modulation type has a strong effect in the amount of harvested energy since the only power source of a passive RFID device is the incident RF power, which must also be used for backscattered communication, thereby making some sort of power loss necessary by definition. This paper defines three metrics to quantify the tradeoffs related to the power/communication quality tradeoffs: M_C defines the percentage modulation depth, which is the communication quality. M_P defines the power harvesting efficiency in percentile terms. M_{Pc} quantifies the power consistency, i.e., the ratio of power received during the transmission of a L or H state. M_{Pc} is an important metric, especially in RFID designs with no buffer, since the power input inequality could cause the IC to lose power and reset itself for low values of M_{Pc}.

Appendix A
Glossary of Terms

In this appendix, we provide a list of the terms and descriptions used in this survey. Table 6 lists the terms used in this survey along with the contexts.

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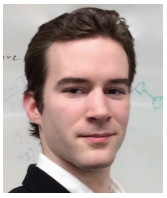

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