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UR-SolarCap: An Open Source Intelligent Auto-Wakeup Solar Energy Harvesting System for Supercapacitor-Based Energy Buffering

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ABSTRACT Energy harvesting systems that couple solar panels with supercapacitor buffers offer an attractive option for powering computational systems deployed in field settings, where power infrastructure is inaccessible. Supercapacitors offer a particularly compelling advantage over electrochemical batteries for such settings because of their ability to survive many more charge–discharge cycles. We share UR-SolarCap—a versatile open source design for such a harvesting system that targets embedded system applications requiring power in the 1–10 W range. Our system is designed for high efficiency and controllability and, importantly, supports auto-wakeup from a state of complete energy depletion. This paper summarizes our design methodology, and the rationale behind our design and configuration decisions. Results from the operation and testing of a system realized with our design demonstrate: 1) an achievable harvester efficiency of 85%; 2) the ability to maintain sustained operation over a two week period when the solar panel and buffer are sized appropriately; and 3) a robust auto-wakeup functionality that resumes system operation upon the availability of harvestable energy after a period in which the system has been forced into a dormant state because of a lack of usable energy. To facilitate the use of the system by researchers exploring embedded system applications in environments that lack a power infrastructure, our designs are available for download as an archive containing design schematics, Printed Circuit Board (PCB) files, firmware code, and a component list for assembly of the system. In addition, a limited number of pre-assembled kits are available upon request.

INDEX TERMS Supercapacitor, energy harvesting, automatic wakeup, solar energy, DC-DC converter, powering embedded systems.

I. INTRODUCTION

Recent years have seen a rising interest in deployments of devices with built-in sensing, computation, and communication capabilities in "field settings" that are characterized by autonomous operation, lack of power infrastructure, and no maintenance. In these situations, either the devices need to be deployed with a sufficient energy source for their operational lifetime or they need to harvest energy from their environment to sustain their operation. Since the availability of the environmental energy is intermittent, energy buffering is also necessary with harvesting. Harvesting has traditionally been considered for rather low-power applications and primarily with rechargeable battery-based buffering.

Low-power (10–100 mW) distributed sensing and communication devices, such as those used in wireless sensor networks (WSNs), already make use of energy harvesting [1], [2], relying on energy sources such as RF (radio-frequency), vibration, and solar radiation [3]–[6]. Low-power sensing and communication platforms utilize low-complexity energy harvesting circuits and methods, such as direct connection of the energy source and buffer [7], [8] and harvesters built upon passive circuit components [9], [10]. The harvesting efficiency of these systems range from 30–65%.

Recent research has focused on more sophisticated embedded systems [11] that run data-intensive applications in the field and require a significant amount of computation for local processing of data to reduce latency, communication bandwidth requirements, and power consumption. Key examples of such systems include those

deployed for computer vision applications such as highway traffic monitoring [12], [13] and for wildlife behavior analysis [14], [15]. Embedded systems such as *BeagleBone Black* [16] and *Arduino Due* [17] can run these applications and consume 1–10 W, which we define as *moderate-power* systems.

For moderate-power systems, solar energy is an attractive choice as an energy source, due to the low cost and ready availability of solar panels [18]. For these systems, although rechargeable batteries represent an extensively-used mature energy buffering technology [19]–[21], supercapacitors provide four significant advantages: i) much higher power density, ii) a virtually infinite lifetime ($\approx 10^6$ charge-discharge cycles) [22], iii) environmentally friendly chemical composition, and iv) better support for precise energy management because of the ability to predict remaining energy with a 2–5% precision [23], [24]. Due to these favorable properties, supercapacitors have been used as the energy buffer for WSNs and low-power embedded systems [7], [25]–[28], as well as moderate-power field systems [29].

Typically, energy harvesting systems use either no active control [21], [27] or a control unit without wakeup capability [26]. As apposed to low-power sensing platforms, energy harvesting for moderate-power systems introduces added design complexity because of the combined requirements of high efficiency ($\geq$80%), software-controllability, and "wakeup" functionality to ensure maintenance-free autonomous operation [30]. The lack of standardized off-the-shelf moderate power harvesters that provide these features, combined with the design complexity of such systems, make their deployment challenging for a large community of researchers.

This paper presents UR-SolarCap, an intelligent open source solar-supercapacitor moderate-power harvester designed at the University of Rochester (UR) for use with commercially available solar panels and supercapacitors. Our design is intended to be usable by a wide range of engineering and sciences research communities because of the combination of (a) intelligent functionality incorporated into our harvester, particularly the auto wakeup, (b) high energy efficiency levels ($\approx$85%) due to a sophisticated and modular circuit design, (c) widespread availability of the inexpensive solar panels, (d) the ability to use supercapacitors in a flexible set of topologies, and (e) minimal expertise required for setup and deployment.

Suitably provisioned, the system can harvest solar energy, buffer it in supercapacitors, and sustain an embedded device through a 5 V regulated voltage output, which is the most common voltage for contemporary embedded systems [16], [31]. The platform consists of internal measurement devices, a low-power microcontroller, and communication interfaces. The system's measurement and communication capabilities provide information on energy availability to the supported embedded system through either its RS-232 port or Bluetooth. This enables the application that is running on the embedded system to implement energy-aware computation techniques to optimize energy usage. Additionally, Bluetooth enabled devices (e.g. smartphones) can obtain information from the system using the Bluetooth interface.

The structure of this paper is as follows: Section II summarizes usage guidelines for the system. Section III describes how the solar panel and supercapacitors can be sized based on application requirements. Section IV describes the modular architecture that realizes the required system functionality. Section V discusses the physical implementation of each system module. Experimental results in Section VI validate system performance. Section VII lists the open resources that we provide and Section VIII concludes the paper.

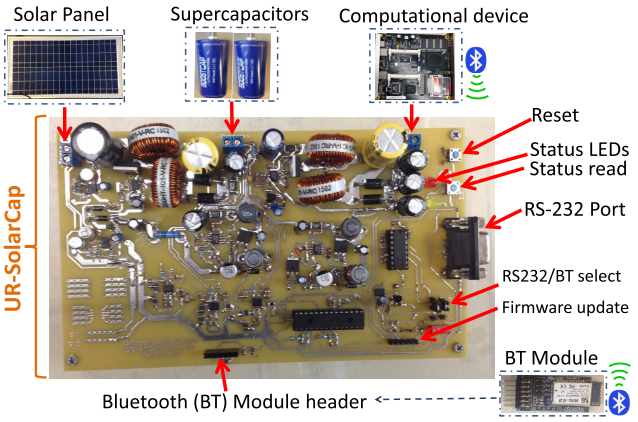


FIGURE 1. The UR-SolarCap system. The system provides power to a 1-10 W computational device once equipped with suitable solar panels and supercapacitors. Key features include auto-wakeup, RS-232 and Bluetooth communication interfaces for smart energy management, system status query button with LED display, system reset, and a firmware update header.

II. SYSTEM USAGE

This section describes the basic functionality of the system as well as the information needed to assemble the overall system. Figure 1 shows the connection interfaces between the UR-SolarCap system and user supplied components. The user-supplied components include:

1) A **Solar Panel** that supplies energy to the system.
2) **Supercapacitors** that buffer energy for the system.
3) A **Computational Device** that is powered by the system. Typically this is an embedded system that runs the application for which the overall system is deployed.
4) An optional **Bluetooth Module** that provides a communication interface for exchanging information with the harvesting system.

The size of the solar panel and size and configuration of the supercapacitors can be chosen by the end user to prioritize cost, footprint, capacity or power, as described subsequently in Section III.

The system operates automatically and autonomously once the solar panel and supercapacitors are connected. Primary control, harvesting, and communication functions of the system are achieved by software running on a microcontroller (μC). Throughout the rest of the

paper, we use the term *firmware* to distinguish this μC software from any application software running on the external computational device. Available solar power from the panel is harvested and buffered in the supercapacitors. When *waking up* from a depleted state, where available energy in the buffer is inadequate for operating the control circuitry, the initial harvesting is passive. Once enough energy is buffered for reliable start-up of the control circuitry, the system transitions to an operational state where it actively manages the energy harvesting to optimize efficiency and controls the availability of power to the computational device. When energy buffered in the supercapacitors is enough to also provide power to the computational device, the system enables the 5 V regulated voltage output for this purpose, while continuing to harvest available solar energy from the panel.

The user can query the status of the system via the "Status read" push button and the two "Status LEDs." The red LED and yellow LED indicate the status as following:

- **Red OFF, yellow OFF:** the system is *depleted* and has insufficient energy to operate.
- **Red ON, yellow OFF:** the system is operating, but the supercapacitor block voltage is less than the minimum 3.6 V required to provide a 5 V output to the computational device. Therefore, the 5 V output is shut off.
- **Red OFF, yellow ON:** the system is operating and supercapacitor block voltage is $\geq$3.6 V and providing 5 V to the computational device, but the supercapacitor block is not fully charged.
- **Red ON, yellow ON:** the supercapacitor block is fully charged. The 5 V output is enabled. Harvesting is intentionally disabled to prevent overcharging the supercapacitors.

In its operational state, the system also measures and reports key operational values, in particular the voltage and current for the terminals connected to the solar panel and the supercapacitors. These values are reported once every three minutes via the RS-232 or the optional Bluetooth interface. The serial "RS-232 Port" is built into UR-Solarcap; Bluetooth requires a separate PmodBT2 Bluetooth module [32] to be connected using the header extension indicated in Fig. 1. The user has the option to select between RS-232 and Bluetooth using the DIP switch and jumpers as shown in Fig. 1.

III. SOLAR PANEL AND SUPERCAPACITOR PROVISIONING

The user must select the size of the solar panel and configuration of the supercapacitors connected to the UR-SolarCap system according to their specific power requirements, the solar radiation availability at the deployment location, and the attributes of the specific panels and supercapacitors used. This section describes this process starting with the commercially advertised parameters used to rate solar panels and supercapacitors that users can readily obtain from manufacturers. For ready reference, Tables 1 and 2 summarize the notational conventions used and the ranges for key system variables that we use in our description.

TABLE 1. Commercially-advertised ratings for the solar panel and supercapacitors and UR-SolarCap provisioning parameters, derived from these ratings.

Value	Description
P_{rated}	Rated power of the solar panel at W_{rated}
W_{rated}	Solar irradiance of 1000 W/m^2 used to rate solar panels
W_{solar}	Solar irradiance to which the solar panel is exposed
V_{rated}	Rated voltage of a single supercapacitor
C_{rated}	Rated capacitance of a single supercapacitor
N_{supercap}	The number of supercapacitors in serial topology
$E_{\text{SC}}^{\text{max}}$	Max. usable energy stored in the supercapacitor block
E_{res}	Unusable (residual) energy in the supercapacitor block
P_{load}	The total power drawn from the supercapacitor block
$t_{\text{down}}^{\text{yr}}$	Average system downtime in hours per year

TABLE 2. Key voltage/current/power variables for the solar panel and supercapacitor block and their minimum and maximum limits determined by the operational limits of the circuit components.

Value	Description	min	max
V_{solar}	Solar panel voltage	6 V	25 V
I_{solar}	Solar panel current	5 mA	2.5 A
P_{solar}	Input solar power to the system	0.1 W	15 W
V_{MPP}	Max. power point voltage of the solar panel	6 V	20 V
V_{SC}	Supercapacitor block voltage	3.6 V	25 V
I_{SCin}	Charging current of the sup. block	0 A	4 A
I_{SCout}	Discharging current of the sup. block	4 mA	3 A

A. SOLAR PANEL SIZING

The solar panel must be provisioned to supply adequate power to the system. Panels are advertised using their rated power, which we denote by P_{rated}. This power is only achievable at a specified rated solar irradiance, W_{rated}. The actual solar irradiance W_{solar} is typically lower than W_{rated} and the actual harvestable power scales approximately linearly with the solar irradiance. Additionally, limits on the harvested power may be specified as an overload protection for the system. We therefore model the actual harvested power as

$$P_{\text{solar}} = \min\left(P_{\text{rated}}\,\frac{W_{\text{solar}}}{W_{\text{rated}}}, P_{\text{Solar}}^{\text{max}}\right), \tag{1}$$

where $P_{\text{Solar}}^{\text{max}}$ is the maximum harvesting limit enforced by the system. Thus, for example, a $P_{\text{rated}} = 30$ W panel, rated at a typical $W_{\text{rated}} = 1000\ W/m^2$ used for rating solar panels [33], will deliver approximately $P_{\text{solar}} = 7.5$ W if the solar irradiance is $W_{\text{solar}} = 250\ W/m^2$ (assuming this is smaller than any system imposed maximum limit).

The solar panel voltage, V_{solar}, and current, I_{solar}, determine the power $P_{\text{solar}} = V_{\text{solar}} \times I_{\text{solar}}$ harvested from the panel. The voltage and current are not independent and their relation is determined by the photodiodes of the solar panel. We treat the voltage V_{solar} as the independent variable that defines the

panel's *operating point* [29], which is tracked and controlled by the system to optimally harvest available solar power. The value of V_{solar} that maximizes P_{solar} is defined as the maximum power point voltage (V_{MPP}) and its range is listed in Table 2. The process by which the μC firmware controls V_{solar} to track V_{MPP} is detailed in Section V-A.

The characteristics of the solar panel also determine permitted configurations that meet the minimum and maximum bounds on V_{solar}, listed in Table 2. The solar panel voltage must be over $V_{\text{solar}}^{\text{min}}$ for the harvester to become operational, and below $V_{\text{solar}}^{\text{max}}$ to avoid hardware damage. By controlling the harvester operating point, the system also limits the harvested power P_{solar} to a maximum value $P_{\text{solar}}^{\text{max}} = 15$ W. This soft limit on the maximum harvested power allows users to provision the solar panel based on periods when solar irradiation is low without having to worry about staying within the operating limits of the components for durations when the solar irradiation is high. Solar panel provisioning is discussed in detail in Section III-C.

B. SUPERCAPACITOR SIZING

The supercapacitor block must be configured to provide adequate energy storage capability. Individual supercapacitors are advertised by their rated capacitance C_{rated} and rated voltage V_{rated}. The supercapacitor block can be configured using fully-parallel, fully-serial or serial-parallel connection topologies [34] provided the operational limits in Table 2 are honored. We consider only a fully-serial configuration, which, as we point out subsequently, is typically desirable. Other configurations, may be similarly analyzed, if required.

For the supercapacitor block, we denote by V_{SC}, I_{SCin}, and I_{SCout} the voltage at the non-grounded terminal, the *charging* current flowing in from the solar panel side, and the *discharging* current flowing out of the supercapacitor into the downstream circuit that powers the harvester control circuitry and the computational device, respectively. Because the harvesting circuitry is unable to extract energy from the supercapacitor block once its terminal voltage drops below a threshold $V_{\text{SC}}^{\text{min}}$, we consider the usable energy stored (at voltage potentials) above this threshold and characterize the storage capability of the supercapacitor block by its maximum usable stored energy, denoted by $E_{\text{SC}}^{\text{max}}$. Storage is limited by the fact that when one attempts to charge supercapacitors above their rated voltage, the excess energy is rapidly lost as heat and therefore not available for use. Prevention from overcharging is also necessary because overcharging can damage the supercapacitors and endanger closeby components and individuals.

Although detailed models for supercapacitor behavior exist [35]–[37], for the purposes of provisioning, an ideal capacitance model is adequate, which estimates the maximum usable buffered energy in the supercapacitor block as

$$E_{\text{SC}}^{\text{max}} = N_{\text{supercap}} \times \tfrac{1}{2}\, C_{\text{rated}}\, V_{\text{rated}}^2 - E_{\text{res}}, \qquad (2)$$

where N_{supercap} is the number of supercapacitors in series; C_{rated} and V_{rated} are the rated capacitance and voltage for each individual supercapacitor; and

$$E_{\text{res}} = \left(\tfrac{1}{2}\, C_{\text{rated}}\, (V_{\text{SC}}^{\text{min}})^2\right) / N_{\text{supercap}} \qquad (3)$$

is the unusable (residual) energy due to the inability to extract buffered energy when $V_{\text{SC}} \leq V_{\text{SC}}^{\text{min}}$. The preceding computation of $E_{\text{SC}}^{\text{max}}$ neglects the impact of any supercapacitor self-discharge because compared to the moderate operating power of the UR-SolarCap harvester, the leakage power (self discharge rate) is negligible [38].

To prevent overcharging, the UR-SolarCap system stops harvesting when the supercapacitor block voltage reaches an upper-limit denoted by $V_{\text{SC}}^{\text{max}}$. A fully-serial connection of the supercapacitors maximizes the supercapacitor block voltage. The fully-serial topology therefore minimizes E_{res} maximizing available energy provided the fully-charged supercapacitor block does not exceeded the maximum limit $V_{\text{SC}}^{\text{max}}$ for V_{SC}. Henceforth, the term "supercapacitor block" refers to this serial configuration in this paper, unless otherwise indicated.

For the experimental configuration used to obtain the results reported in this paper, the various parameters introduced in this section are listed in Table 2 along with their operating limits. The open resources included with the paper (See Section VII) provide multiple firmware versions with pre-selected $V_{\text{SC}}^{\text{max}}$ values ranging between 8.1–24.3 V to minimize the need for users to re-program the firmware. It is also possible to hard-code $V_{\text{SC}}^{\text{max}}$ in the firmware based on the supercapacitor configuration and re-program the microprocessor used in the UR-SolarCap system. Users are strongly advised to read the firmware version selection details in Section VII before making any circuit connections.

C. PROVISIONING OF SOLAR PANEL AND SUPERCAPACITORS

In addition to meeting the min/max constraints listed in Table 2, the chosen solar panel and supercapacitors must supply and store adequate energy to power the desired load. Smaller than necessary solar panels or supercapacitor blocks will cause the system to run out of energy either due to the inability to meet the computational device's power demand or due to an inadequate energy buffer for covering periods of low or no solar availability. These constraints on solar panels and supercapacitors are quantified by considering the average number of hours/year that the system shuts down because it is out of energy, denoted as $t_{\text{down}}^{\text{yr}}$. $t_{\text{down}}^{\text{yr}}$ can be modeled by using information on solar variability available as historically recorded solar irradiance. Specifically, for many locations in the USA, the solar irradiance is available as an average value $W_{\text{solar}}(n)$ over intervals of duration $\Delta t = 1$ hour each [39] for a 20 year duration from 1991 to 2010, where n indexes the hour-long intervals sequentially. Using this data, a corresponding estimate of the harvested power $P_{\text{solar}}(n)$ can be obtained using (1). In turn, the usable energy $E_{\text{SC}}(n)$ and the contribution $\Delta t_{\text{down}}(n)$ to the downtime are computed for

each hourly interval using the following relations:

$$E_{\mathrm{SC}}(n) = \min\left(\max\left(E^0_{\mathrm{SC}}(n), 0\right), E^{\max}_{\mathrm{SC}}\right), \tag{4}$$

$$E^0_{\mathrm{SC}}(n) = E_{\mathrm{SC}}(n-1) + \Delta t\,(P_{\mathrm{solar}}(n) - P_{\mathrm{load}}(n)), \tag{5}$$

$$\Delta t_{\mathrm{down}}(n) = \begin{cases} 0 & E^0_{\mathrm{SC}}(n) \geq 0 \\ \Delta t - \dfrac{E_{\mathrm{SC}}(n-1)}{P_{\mathrm{load}}(n) - P_{\mathrm{solar}}(n)} & E^0_{\mathrm{SC}}(n) < 0, \end{cases} \tag{6}$$

where $P_{\mathrm{load}}(n)$ is the power demanded by the load over the n-th interval including losses and inefficiencies and $E^{\max}_{\mathrm{SC}}$ is the maximum usable energy determined by the supercapacitor block using (2). The average downtime per year is then estimated as

$$t^{\mathrm{yr}}_{\mathrm{down}} = \left(\frac{\sum_n \Delta t_{\mathrm{down}}(n)}{\sum_n \Delta t}\right) \times 365 \times 24. \tag{7}$$

An example plot for the Rochester, NY region for a constant load demand $P_{\mathrm{load}} = 1$ W is provided in Fig. 2 that shows the effect of provisioning on downtime ($t^{\mathrm{yr}}_{\mathrm{down}}$) based on the choice of solar panel P_{rated} on the x axis and supercapacitor $E^{\max}_{\mathrm{SC}}$ on the y axis. Based on such a plot for the chosen location of deployment, a user can select a solar panel and supercapacitor block based on an acceptable hours/year of down time, $t^{\mathrm{yr}}_{\mathrm{down}}$.

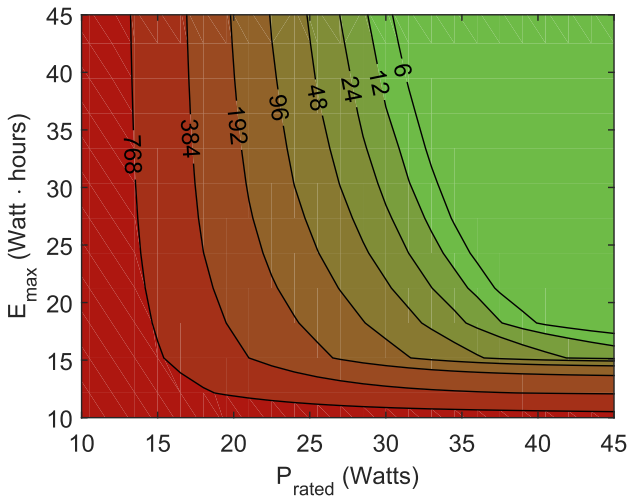


FIGURE 2. Average downtime ($t^{\mathrm{yr}}_{\mathrm{down}}$) in hours per year for a system requiring P_{load} of 1 W. Note that increasing the system's nominal rated solar generation (P_{rated}) or maximum energy storage ($E^{\max}_{\mathrm{SC}}$) decreases $t^{\mathrm{yr}}_{\mathrm{down}}$ as shown by the gradient.

IV. MODULAR ARCHITECTURE

The UR-SolarCap uses a modular architecture with co-designed hardware and software to support autonomous operation, efficiency, controllability, flexibility, and resilience to varying energy availability. Each module, designed to accomplish specific system tasks, is constructed using a combination of the active and passive circuit components which determine its power requirements. In this section, we describe the system modules, the components that make up each module, and the proposed mechanism for intelligently distributing available energy among the modules to achieve self sustainability.

A. SYSTEM MODULES

The **Wakeup Module** allows complete resumption of system functionality from a depleted state. The wakeup module is not firmware-controlled and operates using simple passive circuitry, specifically, uses a DC-DC converter that is directly fed from the solar panel to harvest power. Because the sole focus of this module is a robust wakeup operation, efficiency is not of prime concern and is relatively low. However, the system experiences this low efficiency only until the μC wakes up, at which point, the control circuitry takes over harvesting and the wakeup module is disabled.

The **Control Module** is responsible for active harvesting after the system has woken up and implements the MPPT (Maximum Power Point Tracking) for the solar panel [29] and overcharge protection for the supercapacitor block. The module is implemented in firmware on an 8 bit μC, which provides adequate computation capability for implementing the control tasks and interfaces for the low-level access required for the hardware components in the system. An 8 bit μC consumes less than 10 mW inclusive of interfaces for the peripherals and therefore contributes to high energy efficiency of the harvester in its active operational state. The ability to update the firmware also provides flexibility in modifying the control algorithms.

The **Measurement Module** provides access to the voltage and current values at different points in the system. Harvester control tasks rely on these measurements and some values are also relayed to the computational device for scheduling and coordination purposes. Voltage measurements are readily accomplished using the built-in ADCs (Analog to Digital Converters) in the μC. However, precise current measurements require a specialized CSA (Current Sense Amplifier) IC (integrated circuit) that amplifies small voltage drops (e.g. $<$ 20 mV) across a small sense resistor to levels in the 1–4 V range that can be measured accurately by the μC's ADC.

The **Communication Module** comprises of the RS-232 and Bluetooth communication interfaces. RS-232 communication capability is built into the μC through a UART combined with a ADM232LAN RS-232 level converter IC that generates the $\pm$10 V voltage levels that are required for the RS232 port from the TTL-level 0/5 V signal outputs, generated by the μC. The information transmitted on the RS-232 port (e.g., solar panel voltage V_{solar}) can also be accessed via a USB port on the connecting device using an RS232-to-USB converter cable. Bluetooth is enabled by adding a separate module that implements the Bluetooth stack and interfaces to the μC via its built-in UART.

The **Harvester Module** efficiently transfers solar energy to the supercapacitors. As opposed to the wakeup module that operates passively, the harvester module is actively controlled

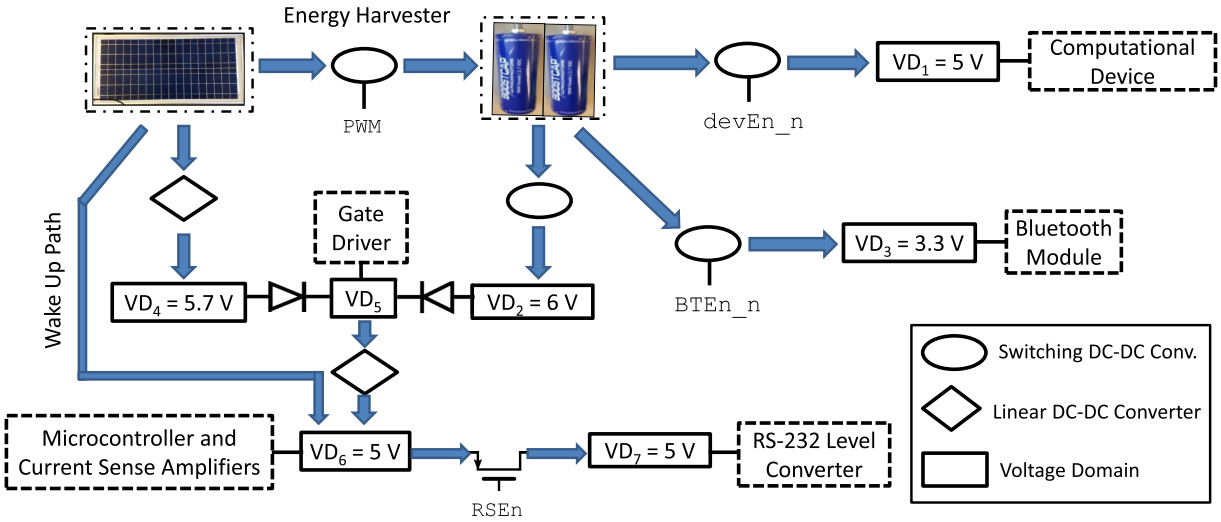


FIGURE 3. Energy distribution among system components through multiple voltage domains (VDs). Arrows show the direction of energy flow through the switching/linear DC-DC converters. The component(s) supplied by each VD are enclosed in a dashed box attached to the domain. The SEPIC architecture of the switching DC-DC converters allow the output voltage to be higher or lower than the input. `PWM`, `devEn_n`, `BTEn_n` and `RSEn` are control signals from the μC. These signals are described in Section V-A and are used to control the harvester and enable/disable VD_1, VD_3, and VD_7, respectively. The wakeup path initiates system operation when the supercapacitors are depleted.

TABLE 3. Active system components and their voltage and current requirements. The Bluetooth module and computational device are external system components. Because our system supplies their operating power they are included in this table.

	Supply Voltage (V)	Current (mA)	Energy Flow Controllability
μC and CSAs	5	2	No
Gate Driver	5–6	0.4 – 6	No
Bluetooth Module	3.3	20 – 30	Yes
RS-232 Level Converter	5	10	Yes
Computational Device	5	$<$ 2000	Yes

by the μC and can only harvest energy when the μC is running. Energy transfer is accomplished using power inductors and a MOSFET driven by a *gate driver* buffer that augments the low current drive capability of the μC.

B. VOLTAGE DOMAINS

Table 3 summarizes the different supply voltage and current requirements for the components that make up the system modules described in Section IV-A. We use multiple *Voltage Domains* (VDs) to allow fine grain control over the energy flow to these components and attain a high overall energy efficiency. The term *Voltage Domain* refers to a voltage-regulated power source that supplies power to a set of system components with similar voltage and current requirements or to another voltage domain. The concept of voltage domains is well established in the field of CMPs (Chip Multiprocessors) as an adaptive energy management approach [40], and in PMICs (Power Management Integrated Circuits) for powering various components of a large system [41].

The voltage domains that constitute our system are shown in Fig. 3. The domains that supply power to the computational device (VD_1), Bluetooth module (VD_3), and the RS-232 level converter (VD_7) are enabled/disabled by the μC. Such ON/OFF control of the VDs allows the μC to achieve high energy efficiency at the expense of increased circuit complexity. The system has three 5 V voltage domains shown as VD_1, VD_6, and VD_7 in Fig. 3. Although they require the same voltage, these three VDs are not merged into a single VD because they have different current and controllability requirements: Both VD_1 (computational device) and VD_7 (RS-232 level converter) require ON/OFF control, whereas VD_6 must always be ON since it feeds the μC. Moreover, VD_1 and VD_6 represent VDs with different current supplies, hence different switching activity levels. Decoupling VD_1 and VD_6 is also in accordance with good design practice to minimize the effects of high switching noise of VD_1 on the measurement circuitry powered by VD_6.

The wakeup functionality is realized by VD_4, which harvests and buffers solar energy in the system when the supercapacitors are too depleted to support active control of harvesting. Initially, when the system starts operation from a depleted state, VD_1, VD_2, and VD_3 are off, since they are fed from the supercapacitor block. When $V_{\text{solar}} \geq V_{\text{solar}}^{\text{min}}$ (6 V as listed in Table 2), VD_4 reaches 5.7 V. As the harvested solar energy increases the supercapacitor block voltage to above the 3.6 V threshold ($V_{\text{SC}}^{\text{min}}$), VD_2 becomes 6 V. By utilizing two diodes, VD_5 is the larger of VD_4 and VD_2, and the wakeup path (VD_4) is automatically *shutting off* when the μC-based controlled harvesting is active.

Excepting VD_5 and VD_7, other VDs are realized using DC-DC converters. The converters themselves are supplied from the solar panel, supercapacitor block, or another voltage domain. VD_7 starts drawing its operating current from VD_6, when a P channel MOSFET ON/OFF switch is turned on by the μC using the `RSEn` control signal (the μC control signals

referred to in this paragraph are described in Section V-A). Two types of DC-DC converters (linear and switching) are utilized to achieve different energy efficiency versus simplicity trade-offs for different parts of the system. Three different types of switching regulators are used: i) an always-active type connecting the supercapacitors to VD_2, ii) a duty-cycle controlled one through the μC's PWM control signal, connected as a harvester, iii) an ON/OFF controlled one through the μC's devEn_n and BTEn_n signals.

Linear regulators are simple and require fewer circuit components than switching regulators, but their efficiency is typically much lower and they only operate when their input voltage is higher than their output. Switching regulators, on the other hand, specifically the SEPIC (Single-Ended Primary Inductance Converter) [42] configurations used in our system, have much higher efficiency and can work under a variety of input/output voltage levels. Because the supercapacitor block operates over a wide voltage range, the VDs that are fed directly from the supercapacitor block are implemented by switching DC-DC converters to achieve high energy efficiency. The design priority for the wakeup module is simplicity and operational robustness. Therefore, this module is implemented by simple passive components and a linear regulator to form VD_4, implying a low efficiency for VD_4. However, the impact of the inefficiency of VD_4 on the overall system efficiency is negligible because VD_4 is turned off most of the time during normal system operation.

V. MODULAR IMPLEMENTATION

Of the five modules described in Section IV-A, the wakeup module is implemented as a voltage domain as described in Section IV-B. In this section, we provide implementation details for the remaining four system modules: control, measurement, communication, and harvester.

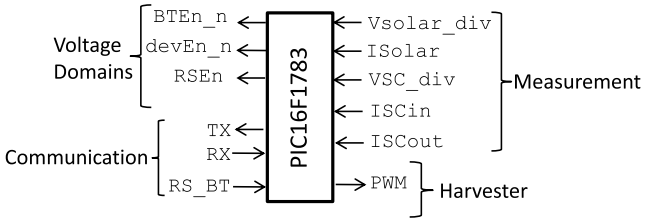


FIGURE 4. The μC's (microcontroller's) hardware interface. The system uses a 10 mW, 8 bit PIC16F1783 μC that incorporates multiple I/O pins and ADC channels. The naming of the signal pins is consistent with the provided firmware code listing.

A. CONTROL MODULE

The control module consists of the μC and the firmware that is loaded in its flash ROM. The input/output (I/O) signals that allow the firmware to interface with the hardware components are shown in Fig. 4 and consist of four groups:

- Measurement: Solar panel voltage (VSolar_div), solar panel current (ISolar), supercapacitor block voltage (VSC_div), supercapacitor input current (ISCin), and supercapacitor output current (ISCout). The firmware accesses these values from the measurement module via the μC's ADC.
- Voltage Domains: The devEn_n, BTEn_n, and RSEn signals allow the microcontroller to enable/disable the voltage domains feeding the computational device (VD_1), Bluetooth module (VD_3), and RS-232 level converter (VD_7), respectively. devEn_n and BTEn_n are active low and RSEn is an active high signal.
- Communication: The TX and RX signals transmit and receive data from either Bluetooth or RS232 communication devices using the RS-232 protocol. Using the jumpers on the board (marked as "RS232/BT select" in Fig. 1), TX and RX pins are multiplexed between the RS232 and Bluetooth devices and the BT_RS signal lets the firmware know which communication method is selected by the user. BT_RS is pulled high (RS-232) or low (Bluetooth), based on the user's selection.
- Harvester: The pulse width modulation (PWM) signal from the μC controls the MOSFET switch of the harvester. Since the current drive capability of the PWM pin is not sufficient (25 mA) to drive the gate of the MOSFET directly, a gate driver is used as a buffer, which allows a drive current of 2 A.

These control signals provide the interface between the firmware in the control module and the hardware components in the other modules. They allow the control algorithms to be implemented in firmware and eliminate the need for hardware modifications when slight adjustments need to be made to the algorithms. Using the signals indicated in Fig. 4, the control module performs the following tasks:

1) MAXIMUM POWER POINT TRACKING (MPPT)

Solar power is harvested using an MPPT algorithm, which must determine a maximum power point, V_{MPP}, for the current solar irradiance (W_{solar}), and control the duty cycle of PWM to keep V_{solar} as close to V_{MPP} as possible. MPPT methods generally rely on single shot or consecutive voltage and current measurements [25], [43] or lookup tables [44]. To capitalize on the flexibility of its μC-based implementation, the UR-SolarCap system uses a firmware implementation of MPPT. Specifically, the fractional open circuit voltage MPPT method [25] is used, which disconnects the solar panel for short intervals to measure the open circuit voltage, V_{OC} and determines V_{MPP} as a constant fraction of the V_{OC} as:

$$V_{MPP} = K \times V_{OC} \tag{8}$$

where K is the constant fraction. Technically, this fraction should be varied depending on the environmental conditions and the characteristics of the solar panel. However, our experiments show that a simple fixed coefficient of $K = 0.82$ produces reasonable MPPT results. Our firmware measures

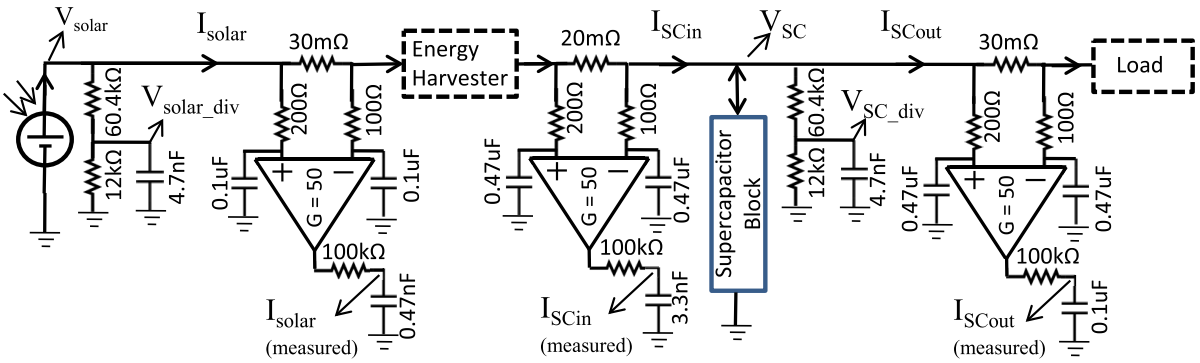


FIGURE 5. Signal conditioning of the voltage and current signals using resistor dividers and CSAs. Based on the configuration, the maximum measurable values of V_{solar}, V_{SC}, I_{solar}, I_{SCin} and I_{SCout} are 24.7 V, 24.7 V, 2.7 A, 4 A, and 2.7 A respectively. The RC branches attenuate the frequency components of the signal which are beyond the 3dB bandwidth of the CSA.

V_{OC} periodically every four minutes. The interval and the constant K are adjustable in the firmware.

2) ENABLING/DISABLING THE VOLTAGE DOMAINS

When the supercapacitor block voltage (V_{SC}) is below V_{SC}^{min} (3.6 V), the firmware disables the voltage domains feeding the computational device (VD_1), the Bluetooth module (VD_3), and the RS-232 converter (VD_7). This threshold voltage is set based on the minimum input voltage of the LTC1624CS8, which is the DC-DC controller IC that receives its input from the supercapacitor block. Even after V_{SC} rises above V_{SC}^{min}, VD_3 and VD_7 are only periodically enabled depending on the selected communication mode as discussed in Section V-C.

3) OVER CHARGE, OVER CURRENT AND OVER POWER PROTECTION

When the solar power, P_{solar}, exceeds 15 W (*over power condition*) or the supercapacitor block charging current, I_{SCin}, exceeds 4 A (*over current condition*), V_{solar} is intentionally increased to a value higher than V_{MPP} to reduce the input power. Once the over current or over power conditions end, V_{solar} is decreased incrementally back down to V_{MPP}. The firmware also protects the supercapacitors from an *over charge condition* by stopping the harvester when V_{SC} reaches its maximum value, V_{SC}^{max}. The maximum value of V_{SC} depends on the number and topology of the supercapacitors, as described previously in Section II. The open-source resources provide six preset maximum V_{SC} values based on the version of the firmware. Firmware version selection details are provided in Section VII.

B. MEASUREMENT MODULE

Figure 5 shows the components of the measurement module. The solar panel voltage (V_{solar}) and supercapacitor block voltage (V_{SC}) are brought into the measurable range using voltage dividers to obtain scaled analog voltage values V_{solar_div}, and V_{SC_div}, respectively, which are measured using the 12 bit, built-in ADC in the μC with a reference voltage of 4095 mV. The solar current (I_{solar}) and the charging and discharging currents I_{SCin} and I_{SCout} for the supercapacitor block are measured in the system. These voltage and current measurements track the amount of energy harvested, buffered, and consumed, as well as the system's efficiency.

The three currents are each measured using a separate MAX4372F CSA (Current Sense Amplifier) which provides a DC gain of 50 V/V with less than 300 μW quiescent power consumption and a 3 dB bandwidth of 200 kHz. Low pass RC filters are used as recommended [45] to smooth out the current signals prior to amplification by each CSA. The low pass filter is especially important for measuring I_{SCin}, as the harvester module's SEPIC architecture charges the supercapacitor block via current pulses whose significant frequency components exceed the 3dB bandwidth of the CSA. To quantify accuracy, the values measured internally by the system were compared against a baseline measured by a DMM (digital multimeter). The results of the comparison, summarized in Table 4, demonstrate maximum deviations of 0.4% for voltage and 5.2% for current measurements.

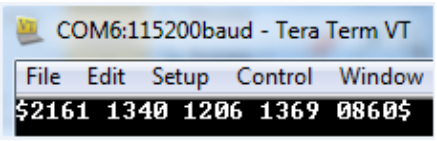


FIGURE 6. A snapshot of the data communicated via the RS-232 serial port. The five values, `VSolar_div`, `ISolar`, `VSC_div`, `ISCin`, `ISCout` are reported between two '$' characters in ASCII format, followed by a line feed (0 x 0A). These values must be multiplied by different scaling factors to obtain actual values.

C. COMMUNICATION MODULE

The communication module transmits a snapshot of instantaneous solar panel voltage (`VSolar_div`), solar panel current (`ISolar`), supercapacitor block voltage (`VSC_div`), charging and discharging currents of supercapacitor block (`ISCin` and `ISCout`) every three minutes. Transmission is in ASCII format to allow quick visualization in a terminal program as shown in Fig. 6. To simplify the firmware code, raw ADC counts are transmitted that can

TABLE 4. Measurement accuracy. The baseline values measured by an Agilent 1272 DMM and the relative deviation for each corresponding internal system measurement are indicated as successive columns proceeding from left to right. To create a more controllable and flexible test scenario, we used a ZUP1624 power supply to emulate solar power. An adjustable power sink is connected to the regulated 5 V to emulate the power consumed by the computational device.

I_{solar} (mA)	Error (%)	V_{solar} (V)	Error (%)	V_{SC} (V)	Error (%)	I_{SCin} (mA)	Error (%)	I_{SCout} (mA)	Error (%)
123	4.8	7.04	0.3	4.03	0.2	396	4.4	98	5.1
211	4.2	8.03	0.3	6.02	0.2	645	4.7	127	5.2
512	5.2	10.04	0.4	8.01	0.2	1108	4.7	228	4.4
684	4.0	12.02	0.4	12.01	0.3	1486	5.1	430	3.5
892	3.1	14.04	0.4	14.02	0.4	2123	5.2	730	2.1
1158	2.0	16.03	0.3	16.02	0.3	2510	5.1	935	2.9
1342	1.7	18.03	0.4	18.00	0.3	2796	3.6	1104	2.7
1489	1.8	20.01	0.4	20.03	0.3	3200	2.8	1327	2.6
1930	1.7	22.03	0.4	22.04	0.2	3405	2.4	1980	1.8
2340	1.8	24.02	0.4	24.07	0.2	3993	2.7	2430	1.9

be scaled to obtain actual values. The scaling factors for `VSolar_div`, (`ISolar`), (`VSC_div`), (`ISCin`, and `ISCout` are 0.006, 0.00067, 0.006, 0.001 and 0.00067, respectively. For example, the ADC value of **2161** for `VSolar_div` corresponds to the voltage $V_{solar} = 2161 \times 0.006 = 12.97$ V. Similarly, **1369** corresponds to the current value `ISCin` $= 1369 \times 0.001 = 1.369$ A.

The communication module provides the hardware interface for either a serial RS-232 connection or a wireless PmodBT2 Bluetooth module. Connecting a Bluetooth module implements the entire Bluetooth stack and acts as a byte pipe with a serial interface to the microcontroller. By default, the PmodBT2 module uses a *slave mode* in which the module is discoverable and waits for an incoming connection. If the control module disables VD_3, and interrupts the module's power supply, the connection must be re-initiated. The Bluetooth module also has an *auto connect mode* where the module itself initiates the connection to another Bluetooth device whose MAC address is internally stored in PmodBT2's firmware. Using this mode, the VD_3 voltage domain can be disabled for arbitrary intervals (to save energy) and the PmodBT2 will automatically initiate a connection whenever it is turned back on. Switching between the slave and auto connect operating modes requires manipulating the PmodBT2's firmware using the provided command interface [46]. To allow the user to flexibly choose between the RS-232 or Bluetooth interfaces, the following communication modes are available:

1) MODE 1 (BLUETOOTH MODULE ON)

In this mode, the VD_3 voltage domain feeding the Bluetooth module is continuously enabled whenever V_{SC} is higher than the 3.6 V threshold. The Bluetooth module can be configured in either slave or auto connect mode; the simplest choice is to leave the module in its default mode (slave) and initiate the connection from the computational device. Since the module operates continuously in this mode, it consumes 100 mW power, which approximately equals the 100 mW power consumption of the rest of system.

2) MODE 2 (DUTY-CYCLED BLUETOOTH COMMUNICATION)

In this mode, the Bluetooth module turns on for a short duration every three minutes, transmits the latest measured voltage and current values, and then turns off. Including appropriate time buffers for initiating the connection and completing the data transmission, this mode has an approximately 5.5% duty cycle, which translates to an average power consumption of ≈6 mW. This power overhead is much lower than that for Mode 1. Similar to Mode 1, the Bluetooth module can be configured in either slave or auto connect mode in Mode 2. Using the auto connect mode eliminates the need for the computational device to poll the Bluetooth device.

3) MODE 3 (DUTY-CYCLED RS-232 COMMUNICATION)

This mode uses the same duty-cycling scheme as Mode 2, but with the wired RS-232 interface as opposed to Bluetooth. Average power consumption in Mode 3 is ≈3 mW. The configuration for the RS-232 communication is 115200 bps, 8 bit, no parity, and no flow control. The RS-232 protocol does not require a connection to be established; therefore, we have not implemented a communication mode in which the RS-232 level converter is continuously enabled (analogous to Mode 1).

To allow rapid deployment without firmware reprogramming, these three proposed communication modes are provided as pre-programmed firmware versions: Set 1 implements Mode 1 and Set 2 implements Modes 2 and 3. In each set, there are multiple firmware versions for different maximum supercapacitor voltage values. If a firmware from Set 2 for duty cycled communication is used, RS-232 or Bluetooth must be selected via the provided DIP switch, whereas the DIP switch has no functionality if a firmware from Set 1 is utilized.

D. HARVESTER MODULE

In the literature, numerous solar energy harvesting designs have been proposed, taking advantage of switching regulator architectures [47]–[49] or switched capacitor

designs [50], [51]. The underlying mechanism of these proposed architectures is to transfer solar energy in consecutive cycles while keeping V_{solar} at the desired maximum power point, V_{MPP}. This guarantees the harvesting of the maximum amount of available solar energy.

Note that the harvested power is independent of the *load*, which is defined as the total power consumption of the system, which is the sum of the power consumption of the computational device and the power overhead of the system. If the load is lower than the available solar power, the excess energy is buffered in the supercapacitors up to their maximum storage capacity. Alternatively, if the load is higher than the available solar power, the required additional power is supplied from the supercapacitors, as part of their buffering functionality.

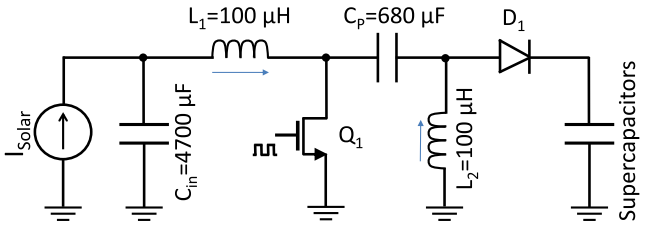


FIGURE 7. Solar-Supercapacitor energy harvester based on SEPIC architecture. A constant current source is used as a simple model for the solar panel's operation around the MPP.

Because the supercapacitor block voltage in our system can be higher or lower than the solar voltage, we use a SEPIC architecture for the harvester [29]. Figure 7 depicts the SEPIC energy harvester topology used in our system which operates at a switching frequency of $f_s = 200$ KHz, corresponding to a cycle time of 5 μs. This circuit harvests energy by transferring a small amount of energy from the solar panel to the supercapacitor block within each 5 μs cycle. Each cycle corresponds to two phases, namely *charge* and *transfer*. The *charge* phase starts when the MOSFET switch Q_1 is turned on. In this phase, the output diode is reverse biased and the supercapacitor block does not receive any energy from the harvester whereas the currents through L_1 and L_2 ramp up (in the directions shown in Fig. 7) increasing the energy stored in these inductors, effectively "charging" them. The *transfer* phase starts when Q_1 is turned off. The output diode D_1 becomes forward biased during this phase and currents through L_1 and L_2 ramp down as energy is transferred from these inductors to the coupling capacitor C_p and the supercapacitor block, respectively.

The SEPIC transfers energy to the supercapacitors in discontinuous mode, controlled by a single duty-cycle parameter D, which is the ratio of the charge phase duration to the cycle time. Ignoring circuit losses for simplified analysis, the input and output voltages in a typical SEPIC configuration are

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D}{1-D}. \tag{9}$$

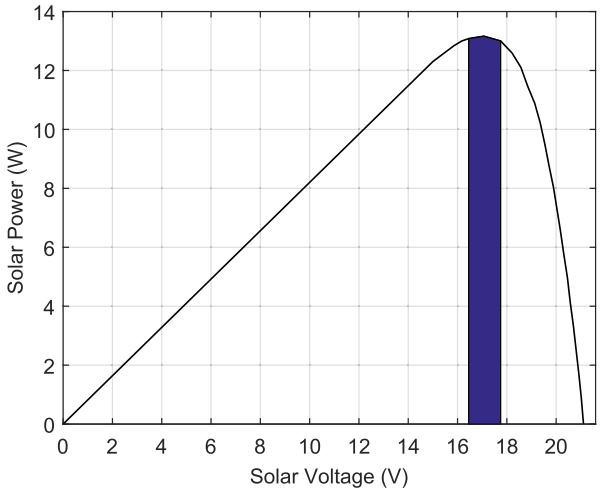


FIGURE 8. Harvested solar power at different V_{solar} values. The shaded area corresponds to the operating range where over 98% of the available solar power is harvested.

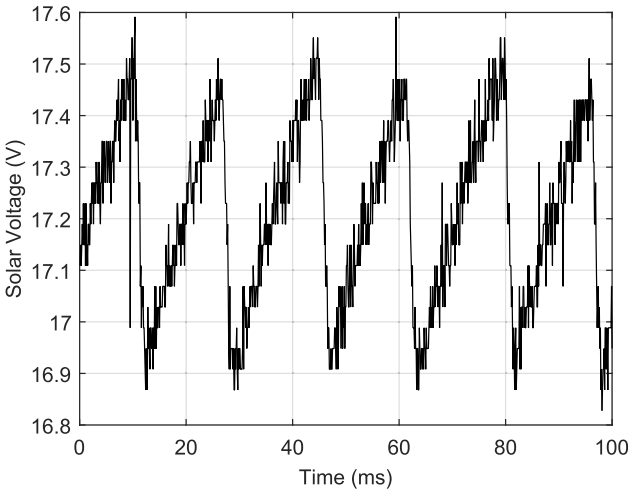


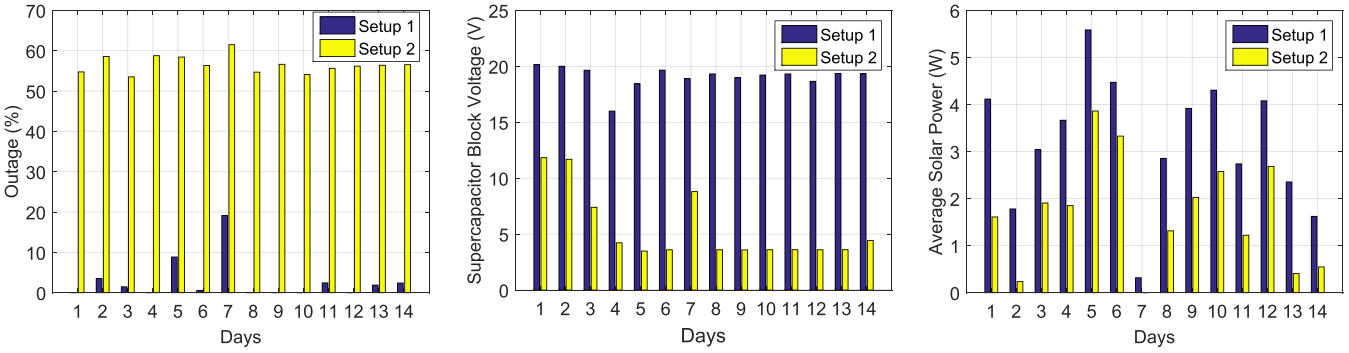
FIGURE 9. A trace of the solar panel voltage V_{solar} over a duration where the harvester control is targeting the maximum power operating point $V_{\text{MPP}} = 0.82 \times 21\ V = 17.2\ V$, where the open circuit voltage is 21 V. The plot corresponds to $P_{\text{solar}} = 13\ W$ and $V_{\text{SC}} = 19\ V$. In practice, V_{solar} varies between 16.9 V and 17.6 V and ensures the harvesting of over 98% of the maximum available solar power, as shown in Fig. 8.

The ability for the SEPIC configuration to control the energy transfer through the adjustment of a single value D for any combination of input and output voltages makes it a good choice for our system. However, the harvester's ability to keep the solar voltage close to V_{MPP} is quite sensitive to the resolution of the `PWM` signal of the μC. The firmware-generated `PWM` signal of the PIC16F1783 μC allows the `PWM` duty cycle D to be controlled in 2.5% increments, which provides a reasonable control of the operating point for our purposes.

Conventionally, the SEPIC is used as a versatile DC-DC converter by selecting the duty cycle D in (9) to provide a regulated constant output voltage V_{out} under varying conditions of the input voltage V_{in}, which may be

TABLE 5. Configuration of the two different experimental setups, tested over the same 14-day duration. Setup 1 and Setup 2 both use Maxwell BoostCap series supercapacitors [53] with a maximum rated voltage $V_{rated} = 2.7$ V per supercapacitor.

	Setup 1	Setup 2
Solar Panel	30 W	2×10 W in parallel
Supercapacitor Block	8×3000 F in series	8×350 F in series
Max. Usable Energy (E_{SC}^{max})	23.6 Wh	2.76 Wh
Communication Method	Duty Cycled RS-232 (Mode 3)	Duty Cycled Bluetooth (Mode 2)
Load Emulating the Computational Device	3 W between 8 AM - 8 PM 1 W between 8 PM - 8 AM	Continuous 2 W



(a) Outage. (b) V_{SC} at the end of the day (8 PM). (c) Average P_{solar} between 9 AM-11 AM.

FIGURE 10. Summary statistics for the experiment conducted with the two setups during the 14-day experiment. (a) Outage percentage. (b) The supercapacitor voltage V_{SC} at the 8 PM each day that approximately indicates the available buffered energy at the end of the duration of sunlight. (c) Average solar power P_{solar} between 9 AM-11 AM, used as an indicator of each day's general solar conditions. The 9 AM - 11 AM period is used because for sunny days, the supercapacitor block is typically fully charged after 11 AM in Setup 2 and the reported solar voltage and current do not represent the *available* solar power beyond this time.

higher or lower than the desired output voltage. The UR-SolarCap harvester configuration differs from the conventional setting because the SEPIC output voltage, i.e. the supercapacitor block terminal voltage, is not constant. However, the operating principle of SEPIC remains unchanged and appropriate selection of the duty cycle D allows transfer of harvested energy from the solar panel into the supercapacitor block, irrespective of whether the input voltage V_{solar} from the solar panel is above or below the voltage V_{SC} for the supercapacitor block. The UR-SolarCap harvester is designed to meet the following constraints:

$$\begin{aligned} P_{Solar}^{max} &= 15\ W, \\ 6\ V &< V_{solar} < 25\ V, \\ 6\ V &< V_{MPP} < 20\ V, \\ 3.6\ V &< V_{SC} < 25\ V, \\ f_s &= 200\ kHz. \end{aligned} \tag{10}$$

The circuit components used in our harvester design are selected to meet these constraints based on industrial application notes [42], [52]. The constraints in (10) imply a maximum supercapacitor charging current of ≈4 A when harvesting the maximum solar power (P_{solar}) of 15 W with the supercapacitor block at its lowest voltage of 3.6 V. The firmware limits the charging current at 4 A, allowing the harvester to also function when the supercapacitor block voltage (V_{SC}) falls below 3.6 V.

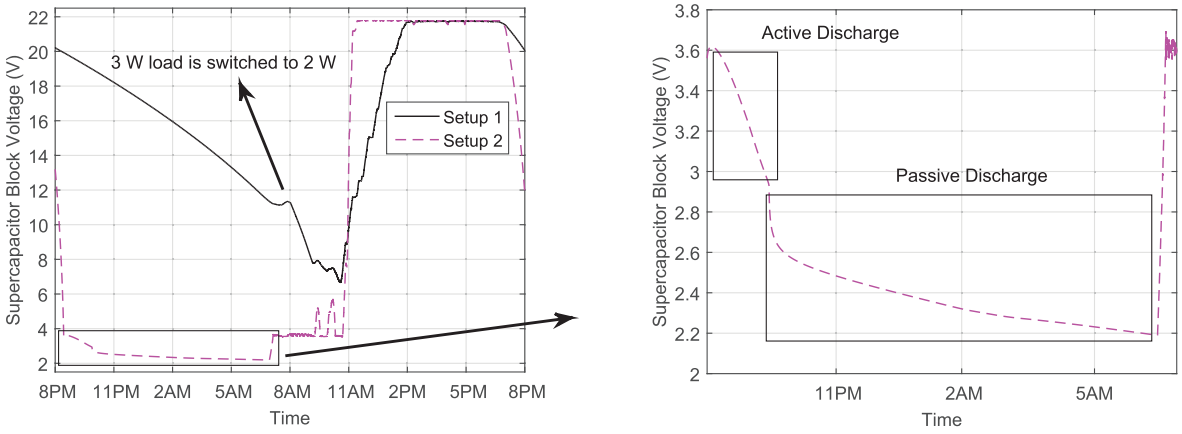
The harvester's firmware keeps V_{solar} as close to V_{MPP} as possible by making periodic adjustments to the duty cycle D of the `PWM` signal. Since the V_{solar} and V_{MPP} change rapidly during the course of harvesting, V_{solar} exhibits small variations around V_{MPP}. The ability of the harvester to closely track V_{MPP} depends on the resolution of the `PWM` signal, as previously mentioned. As shown in Fig. 9, V_{solar} varies in an approximately periodic pattern with a fundamental frequency that is much lower than the switching frequency (f_s). By mapping the range of variation in Fig. 9 to the abscissa (x-axis) of Fig. 8, we can see that despite the variation in V_{solar}, the SEPIC manages to harvest over 98% of the maximum extractable energy at optimal operating point V_{MPP}, which is more than adequate for our design purposes.

VI. EXPERIMENTS

In this section, we present experimental results that verify three major design goals of the UR-SolarCap system: i) robust and sustainable operation, ii) wakeup operation, and iii) high energy efficiency.

A. ROBUST AND SUSTAINABLE OPERATION

In order to verify robust operation over an extended period of time, two parallel experiments were conducted over the course of 14 consecutive days, configured as listed in Table 5 as Setup 1 and Setup 2. Setup 1 demonstrates the ability



(a) Supercapacitor block voltage recorded over 24-hours.

(b) Internal discharge after the load is disabled.

FIGURE 11. A trace of the supercapacitor block voltage (V_{SC}) for Setup 1 and 2 over a 24-hour (night-day) period. The area enclosed by the rectangle in subfigure (a) corresponds to the duration over which the system of Setup 2 is not supplying power to the computational device because of low buffered energy. This region, magnified in subfigure (b), further shows two subregions: the first (labeled active discharge) over which the harvester control circuitry is operational and the second (labeled passive discharge) over which the control circuitry is inoperational due to inadequate power.

to support continuous operation and is provisioned with a 30 W solar panel ($P_{\text{rated}} = 30$ W) and eight serially connected 3000 F Maxwell BoostCap supercapacitors to provide $E_{\text{SC}}^{\max} = 23.6$ Wh, according to the provisioning guidelines detailed in Section III. Setup 2 demonstrates UR-SolarCap's robust wakeup functionality and is provisioned to run out of energy each night. Therefore, a 20 W solar panel and a much smaller supercapacitor buffer of $E_{\text{SC}}^{\max} = 2.76$ Wh are used for this setup. Each day Setup 2 must resume operation from a depleted state, where the system has no usable energy.

System performance during the 14 days is represented using three measures: i) outage (%), ii) supercapacitor block voltage (V_{SC}) at the end of the day, and iii) the daily solar power (P_{solar}) averaged between 9 AM-11 AM. *Outage* is quantified as the percentage of time that the load does not receive the 5V regulated supply during the 24-hour period. In addition to the communication module, during the 14 day experiment, an independent logger also recorded V_{solar}, V_{SC}, and the supply voltages of the computational device and μC. This data is available even when the communication module is disabled due to lack of usable energy.

As shown in Fig. 10, Setup 1 maintains a low outage percentage, and Setup 2 successfully wakes up and operates for at least 35% of each 24 hour duration. The outage percentage in Setup 1 is under 4% except for day 5 and day 7. Increased outage during day 5 is due to the fact that the supercapacitors were not fully charged at the end of day 4 and were depleted well before the sunrise on day 5. On day 7, P_{solar} was very low due to cloudy weather, causing the much higher than typical outage for Setup 1.

As the ratio of the solar panels' size in the two setups is 2/3, we expect a similar ratio between P_{solar} harvested by each setup in Fig. 10c. However, Setup 2 occasionally runs out of energy in the morning and the solar power is not recorded in these outage intervals; this missing data is deemed zero for the

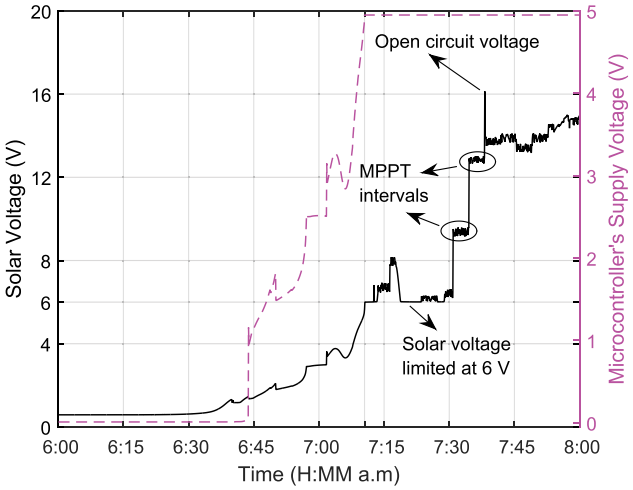
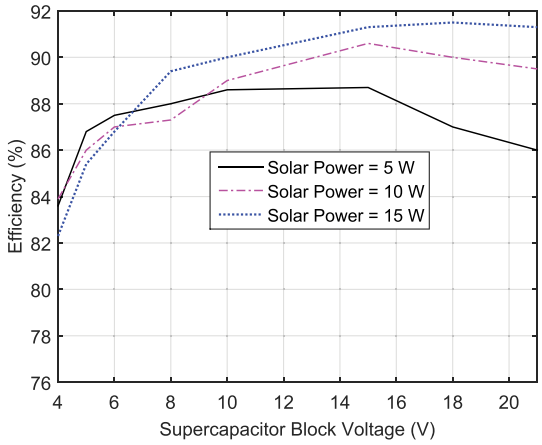


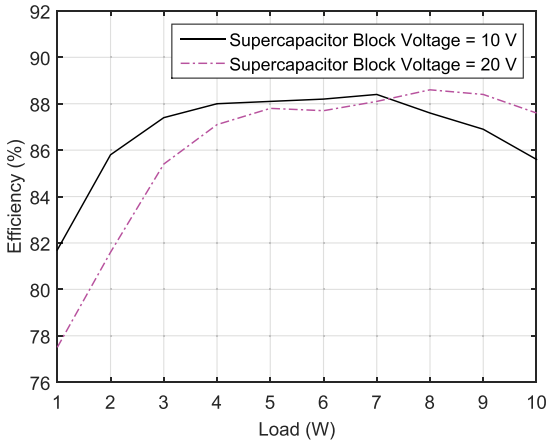
FIGURE 12. A trace of the solar panel voltage V_{solar} (*left axis*) and the microcontroller supply voltage (*right axis*) over a morning epoch demonstrating the UR-SolarCap wakeup functionality starting from a depleted state. Before the time instant indicated by the vertical line at approx. 7:10 AM, because there is inadequate power, the control circuitry is inactive and harvesting is passive. Beyond this time instant (after 7:10 AM) the control circuitry is active and harvesting is active and tracks the MPPT. For occasional short duration intervals after 7:10 AM, insufficient solar power causes the solar voltage to fall below 6 V, and the firmware stops active harvesting to prevent unstable operation. Two sample MPPT intervals occurring after 7:30 AM are encircled.

computations, causing the ratio to deviate significantly from 2/3 for day 2 and day 13.

Figure 11a presents an informative view of the operation of the two systems over a typical sunny day by showing a trace of the supercapacitor block voltage (V_{SC}) over a 24 hour period. From the figure, one can see that V_{SC} for Setup 1 is always above 3.6 V, demonstrating this setup's potential to continuously supply power with no outage. Note that the sharp change in the rate of discharge of V_{SC} at 8 AM is due to switching of the load power P_{load} from 1 W to 3 W.



(a) Harvester efficiency vs. supercapacitor block voltage. The experiment is done at $V_{solar} = 15$ V. A ZUP1624 power supply is used to emulate available solar power.



(b) 5 V regulator efficiency vs. emulated load. A controllable power sink is utilized to emulate the power consumption of the computational device.

FIGURE 13. Energy efficiency of the harvester (a) and the 5 V regulator that feeds the computational device (b). A block of serially-connected 8×3000 F supercapacitors with a rated voltage $V_{rated} = 2.7$ V is used in the experiment.

For Setup 2, V_{SC} rapidly decreases to 3.6 V after sunset as the 2 W load consumes the usable buffered energy.

After V_{SC} falls below 3.6 V and the computational device supply voltage is disabled, the system's internal power consumption discharges the supercapacitors. This discharge pattern continues until V_{SC} reaches 2.9 V. We call this region *active discharge* (2.9–3.6 V), where the components are still running and consuming power. When V_{SC} falls below 2.9 V, the regulator which creates VD_2 loses regulation and the components fed by that domain stop consuming power. However, the quiescent power consumption of the regulators fed by the supercapacitor block cause V_{SC} to decrease at a reduced slope (*passive discharge*). The supercapacitors continued to discharge until 7 AM when the system wakes up and resumes operation. Figure 11b is a magnified version of the 8 PM-8 AM portion of Fig. 11a, where active and passive discharge occurs.

B. WAKEUP OPERATION

Although Setup 2 already demonstrated the robust wakeup capability of UR-SolarCap over the 14 day operaion shown in Fig. 10, we also conducted an additional experiment to highlight the wakeup process in greater detail. Specifically, to examine the wakeup function, the experiment was initiated in the night by connecting the UR-SolarCap harvester to a fully depleted 8×350 F supercapacitor block (eight serially-connected 350 F supercapacitors) and a 30 W solar panel. Solar voltage (V_{solar}) and the voltage domain feeding the μC (VD_6) were logged every 5 s using the independent logger. As mentioned in Section IV, VD_4 (5.7 V) initiates the wakeup operation. This requires the V_{solar} to exceed 5.7 V plus the dropout voltage of the regulator (≈0.2 V). After the system wakes up, tasks such as MPPT and energy harvesting resume.

Figure 12 shows the obtained results during the 6 AM-8 AM time interval. The regulator which generates VD_6 is totally shut down until 6:45 AM. When the solar voltage exceeds 1.4 V, the regulator turns on and starts to follow the solar voltage. When the solar voltage exceeds 6 V, VD_6 increased to 5 V and the μC woke up. The solar voltage continues to increase between two consecutive MPPT intervals after 7:30 AM, as the solar power increases.

C. ENERGY EFFICIENCY

Due to the power loss caused by the circuit components of the harvester, the 5 V regulator, and the μC, not all of the available solar energy is delivered to the computational device. In order to quantify the energy efficiency of the system, a separate experiment is contucted to measure the efficiency of the harvester and the 5 V regulator separately. The results are shown in Fig. 13. Note that as the efficiency is measured based on the total power delivered to or drawn from the supercapacitor block, the contribution of system's internal power consumption is already included in the efficiency numbers.

Figure 13a depicts harvester's efficiency vs. supercapacitor block voltage for three different solar power values (5 W, 10 W, and 15 W). The relatively low efficiency at low supercapacitor voltages is due to the ohmic losses experienced in the system resulting from higher operating currents to deliver the same amount of output power. These ohmic losses are caused by the winding resistance of the inductors (≈20–30 mΩ), the ON resistance of the switching MOSFETs (≈10 mΩ), and the Equivalent Series Resistance (ESR) of the coupling capacitor (≈50 mΩ). The efficiency increases as the supercapacitor block voltage increases up to 15-18 V. Beyond this voltage, the efficiency decreases slightly due to the higher quiescent power consumption of the system at these higher supercapacitor block voltages.

Figure 13b depicts the efficiency of the 5 V voltage regulator at two different supercapacitor block voltages (10 V and 20 V). In both cases, the regulator's efficiency is

lower at light loads (1–3 W) due to the contribution of internal system power consumption. An almost constant efficiency is observed above 3 W for both cases. Only for the lower supercapacitor voltage case (10 V), a slight drop in efficiency is observed at high loads ($\geq$7 W) due to the ohmic losses. In both cases, the efficiency is between 78–88%.

VII. OPEN RESOURCES

The different parts of the system described in this paper are available as open-source documents. Furthermore, a limited number of assembled boards are available as an unrestricted gift to academic institutions upon approval of a research proposal. The open resources contain the hardware and software design of the system and are categorized as follows:

1) **PCB and Schematic:** The PCB and the circuit schematic of the system are designed using Ultiboard and Multisim 13 software. The project files, PCB Gerber files, and a PDF version of the schematics are available.
2) **Component List:** We have provided a part number list of the circuit components that are used in the system. We have used off the shelf components that can be readily purchased from Digikey.
3) **Microcontroller Firmware:** The microcontroller firmware is written using the C programming language and the MikroC coding environment. The project files containing the source code and the HEX file of the firmware are available. Two sets of firmware versions are provided in which Set 1 implements the communication Mode 1 and Set 2 implements communication Mode 2 and 3. In each set, six firmware versions are included to internally limit the supercapacitor block voltage at 8.1, 13.5, 16.2, 18.9, 21.6 and 24.3 V.

A web page for the system is created where the open resources are provided. The web page can be accessed as: http://www.ece.rochester.edu/projects/siplab/OpenWare/UR-SolarCap.html

VIII. CONCLUSIONS

In this paper, an open-source energy harvesting system is presented, which uses solar panels as its sole energy input and supercapacitors as its sole energy buffer. The system is able to harvest a maximum solar power of 15 W and provide a regulated 5 V voltage to an external embedded device (termed *computational device* throughout the paper) that has a maximum power consumption of 10 W. Designed to operate in harsh environmental conditions where the solar energy might be absent for extended periods of time, the system is able to wakeup and resume functionality from a fully-depleted state, when the supercapacitors have zero remaining energy. During its normal operation, the system uses its built-in RS-232 or Bluetooth communication capability to transmit vital energy-state information to the external computational device. Such information includes the solar voltage, supercapacitor block voltage, solar current, and supercapacitor charge/discharge currents. Using this information, the embedded device could make software-level decisions to maximize its energy efficiency by intelligently using different software components, corresponding to different energy consumption levels.

The circuit design and operational details of the system are provided in detail. The harvesting and measurement functionality of the system are achieved via a microcontroller (μC)-based design; solar energy harvesting algorithms such as Maximum Power Point Tracking (MPPT) are the responsibility of the μC software (termed *firmware* throughout the paper). To achieve high efficiency levels, the system is designed as a fine-granularity modular architecture; multiple *voltage domains* are implemented that provide optimum voltage levels to different modules of the system. Some of these voltage domains are always active when the system is awake, while some of them are controlled by the μC to enable/disable the power hungry domains and implement intelligent energy saving methods. Extensive experiments demonstrate the robustness of system operation and an average harvesting efficiency of 80–85%. The schematics, PCB drawings, and the firmware code of the system are provided as open-source documents to allow quick deployment by other researchers.

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